Datasheet

APM32F051x6x8

Arm® Cortex® -M0+ based 32-bit MCU

Version: V1.8

1 Product characteristics

System architecture
- 32-bit Arm® Cortex ® -M0+ core
- Up to 48MHz working frequency

Memory
- Flash: 32~64KB
- SRAM：8KB

Clock
- 4~32MHz crystal oscillator
- RTC 32KHz oscillator with calibration
- Internal 40KHz RC oscillator
- Internal 8MHz RC oscillator
- PLL supports 6 times of frequency

Reset and power management
- Digital and I/O power supply voltage: V_{DD}=2.0~3.6V
- Analog power supply voltage: V_{DDA} = V_{DD} ~3.6V
- Power-on/power-down reset (POR/PDR)
- Programmable power supply voltage detector (PVD) supported
- Support external battery VBAT as power supply of RTC and backup register: V_{BAT}=1.65~3.6V

Low-power mode
- Sleep, stop and standby

Up to 55 fast I/O pins
- Support all mappable external interrupt vectors
- Up to 36 I/Os have 5V fault tolerance

5-channel DMA controller

Analog peripherals
- 1 12-bit ADC; up to 16 external channels supported, conversion range: 0 ~ 3.6V, independent analog power supply: 2.4~3.6V
- 1 12-bit DAC
- 2 programmable analog comparators
- Up to 18 capacitive sensing channels, supporting touch, linear and rotation touch sensors

Timer
- 1 16-bit advanced control timer that can provide up to 7-channel PWM output, support dead zone generation and braking input functions
- 1 32-bit and 5 16-bit general-purpose timers, each with up to 4 independent channels to support input capture/output comparison, PWM complementation, infrared control decoding or DAC control.
- 1 16-bit basic timer
- 1 independent watchdog and 1 system window watchdog timer
- 1 system tick timer

RTC
- Support calendar function
- Alarm and regular wake-up from stop/standby mode

Communication interface
- 2 I2C interfaces; one supports ultra fast speed (1Mbit/s) and SMBus/PMBus and wake-up
- 2 USART interfaces, all support master synchronous SPI and modem control, one of which supports ISO7816 interface, LIN, IrDA interface, automatic baud rate detection and wake-up
- 2 SPI interfaces (18Mbit/s), one supports I2S interface multiplexing
- 1 HDMI CEC interface, woken up on receiving at the first time

CRC computing unit

Serial wire debugging (SWD)

96-bit UID

Contents

2 Product information

See the following table for APM32F051x6x8 product functions and peripheral configuration.

Table 1 Functions and Peripherals of APM32F051x6x8 Series Chips

Product		**APM32F051xx**									
Model		**K6**	**K8**	**C6**	**C8**	**K6**	**K8**	**C6**	**C8**	**R6**	**R8**
Package		**QFN32**		**QFN48**		**LQFP32**		**LQFP48**		**LQFP64**	
Core and maximum working frequency		Arm® 32-bit Cortex®-M0+@48MHz									
Operating voltage		2.0~3.6V									
Flash (KB)		32	64	32	64	32	64	32	64	32	64
SRAM(KB)		8									
Timer	16-bit general	5									
	32-bit general	1									
	16-bit advanced	1									
	16-bit basic	1									
	System tick timer	1									
	Watchdog	2									
Real-time clock		1									
Communication interface	USART	2									
	SPI/I2S	1(1)/1			2/1	1(1)/1			2/1		
	I2C	1(2)			2	1(2)			2		
12-bit ADC	Unit	1									
	External channel	10								16	
	Internal channel	3									
12-bit DAC	Unit	1									
	Channel	1									
GPIOs		27		39		25		39		55	
Analog comparator		2									
Operating temperature		Ambient temperature: -40℃ to 85℃/-40℃ to 105℃ Junction temperature: -40℃ to 105℃/-40℃ to 125℃									

Note:

(1) SPI2 does not exist.

(2) I2C2 does not exist.

3 Pin information

3.1 Pin distribution

Figure 1 Distribution Diagram of APM32F051x6x8 Series LQFP64 Pins

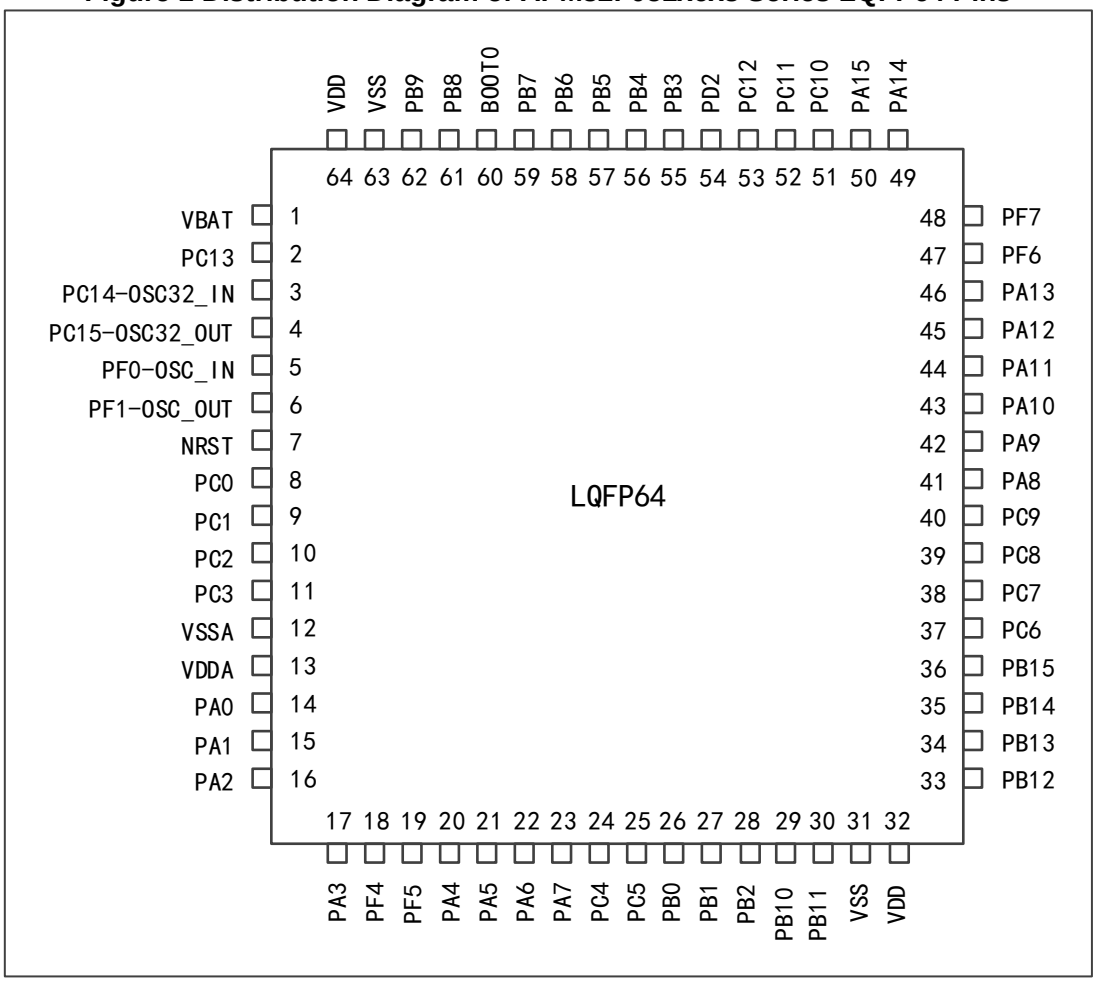


Figure 2 Distribution Diagram of APM32F051x6x8 Series LQFP48 Pins

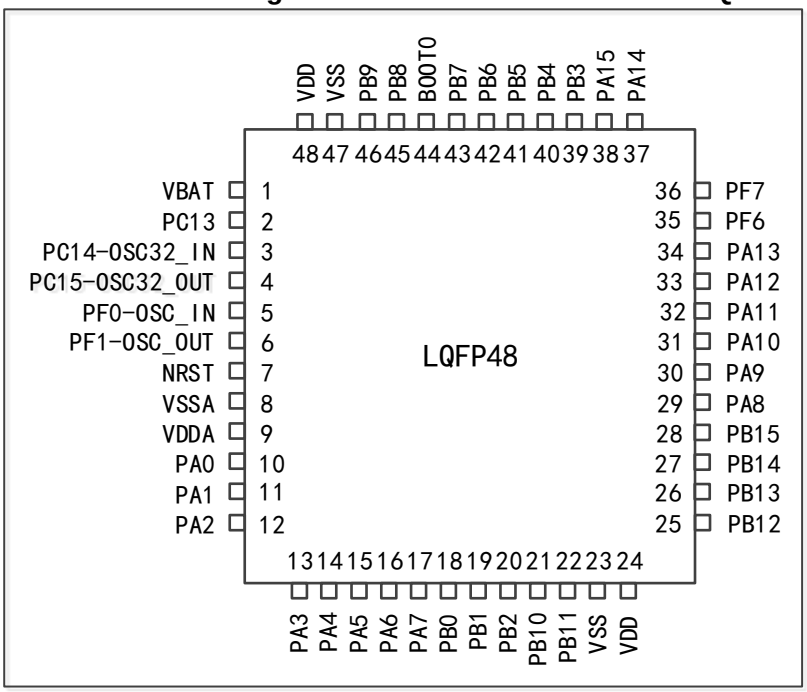


Figure 3 Distribution Diagram of APM32F051x6x8 Series LQFP32 Pins

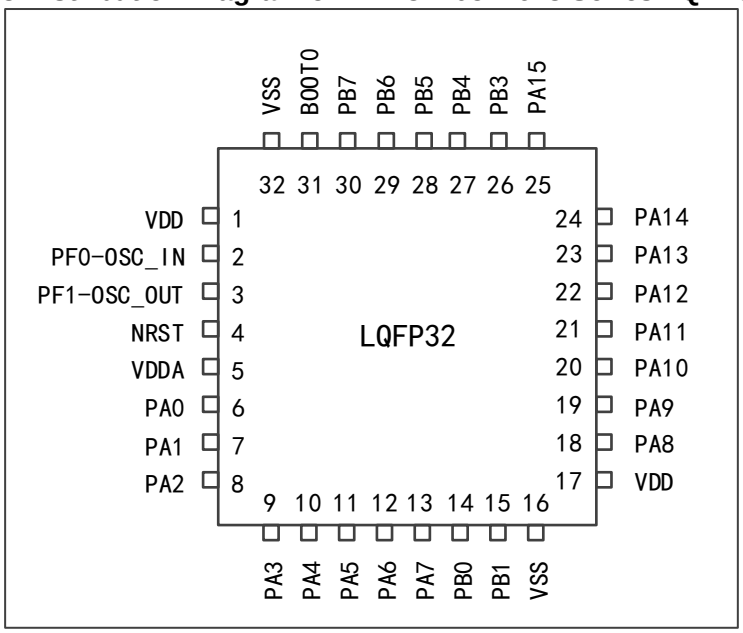


Figure 4 Distribution Diagram of APM32F051x6x8 Series QFN48 Pins

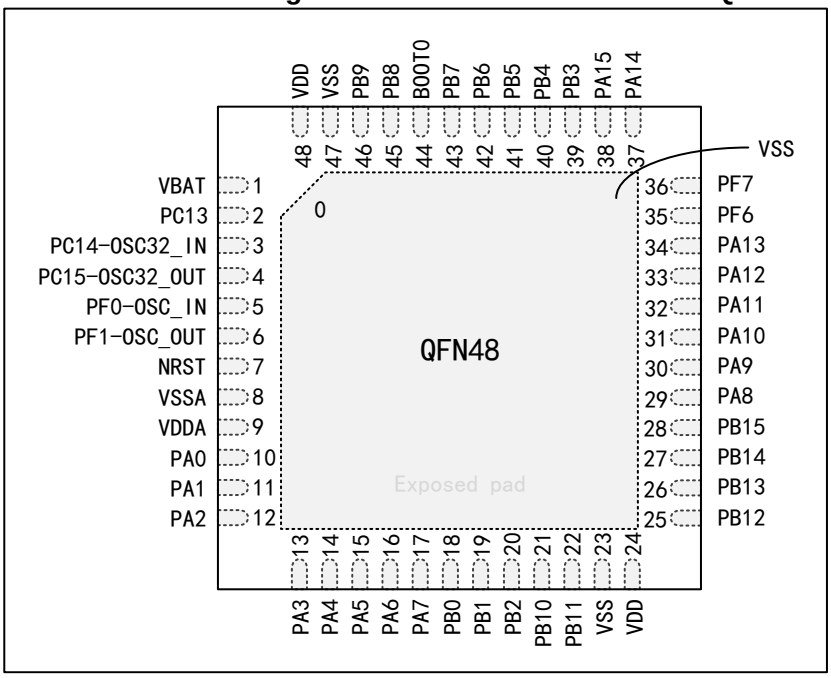
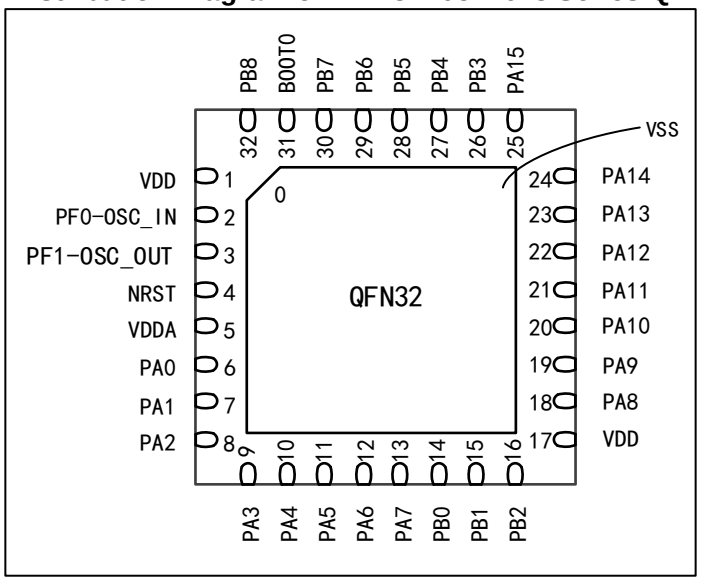


Figure 5 Distribution Diagram of APM32F051x6x8 Series QFN32 Pins



3.2 Pin function description

Pin name: The pin functions during and after reset are the same as the actual pin name (unless otherwise specified in parentheses below the pin name).

Table 2 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin type	S	Power pin
	I	Only input pin
	I/O	I/O pin
I/O structure	TC	Standard 3.3VI/O
	TTa	I/O with 3.3 V tolerance, directly connected to ADC
	FT	FT I/O
	FTf	I/O, FM+ function with 5 V tolerance (ultra fast speed I2C I/O)
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with built-in weak pull-up resistor
Multiplexing function	Functions controlled by GPIOx_AFR register; Configure GPIOx_AFR register to start the corresponding function	
Additional function	Functions directly controlled through peripheral registers; configure peripheral registers to start the corresponding function	

Note: All I/Os are floating input during and after reset (unless otherwise specified).

Table 3 APM32F051x6x8 Pin Function Description

Pin name (Function after reset)	Pin code				Pin Type	I/O Structure	Note	Pin function	
	LQFP 64	LQFP48/QFN48	LQFP 32	QFN 32				Multiplexing function	Additional function
V_{BAT}	1	1	-	-	S	-	-	Backup power supply	
PC13	2	2	-	-	I/O	TC	(1)	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
PC14-OSC32_IN (PC14)	3	3	-	-	I/O	TC	(1)	-	OSC32_IN
PC15-OSC32_OUT (PC15)	4	4	-	-	I/O	TC	(1)	-	OSC32_OUT
PF0-OSC_IN (PF0)	5	5	2	2	I/O	FT	-		OSC_IN
PF1-OSC_OUT (PF1)	6	6	3	3	I/O	FT	-	-	OSC_OUT
NRST	7	7	4	4	I/O	RST	-	Chip reset input/internal reset output (active low)	
PC0	8	-	-	-	I/O	TTa	-	EVENTOUT	ADC_IN10
PC1	9	-	-	-	I/O	TTa	-	EVENTOUT,	ADC_IN11
PC2	10	-	-	-	I/O	TTa	-	EVENTOUT	ADC_IN12
PC3	11	-	-	-	I/O	TTa	-	EVENTOUT	ADC_IN13
V_{SSA}	12	8	-	0	S	-	-	Analog ground	
V_{DDA}	13	9	5	5	S	-	-	Analog power supply	
PA0	14	10	6	6	I/O	TTa	-	USART2_CTS, TMR2_CH1_ETR, COMP1_OUT, TSC_G1_IO1	ADC_IN0, COMP1_INM6, RTC_TAMP2, WKUP1
PA1	15	11	7	7	I/O	TTa	-	USART2_RTS, TMR2_CH2, TSC_G1_IO2, EVENTOUT	ADC_IN1, COMP1_INP
PA2	16	12	8	8	I/O	TTa	-	USART2_TX, TMR2_CH3, TMR15_CH1, COMP2_OUT, TSC_G1_IO3	ADC_IN2, COMP2_INM6
PA3	17	13	9	9	I/O	TTa	-	USART2_RX, TMR2_CH4, TMR15_CH2, TSC_G1_IO4	ADC_IN3, COMP2_INP
PF4	18	-	-	-	I/O	FT	-	EVENTOUT	-
PF5	19	-	-	-	I/O	FT	-	EVENTOUT	-
PA4	20	14	10	10	I/O	TTa	-	SPI1_NSS, I2S1_WS, USART2_CK, TMR14_CH1, TSC_G2_IO1	ADC_IN4, COMP1_INM4, COMP2_INM4, DAC_OUT1
PA5	21	15	11	11	I/O	TTa	-	SPI1_SCK, I2S1_CK, CEC, TMR2_CH1_ETR, TSC_G2_IO2	ADC_IN5, COMP1_INM5, COMP2_INM5

Pin name (Function after reset)	Pin code				Pin Type	I/O Structure	Note	Pin function	
	LQFP 64	LQFP48/QFN48	LQFP 32	QFN 32				Multiplexing function	Additional function
PA6	22	16	12	12	I/O	TTa	-	SPI1_MISO, I2S1_MCK, TMR3_CH1, TMR1_BKIN, TMR16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT	ADC_IN6
PA7	23	17	13	13	I/O	TTa	-	SPI1_MOSI, I2S1_SD, TMR3_CH2, TMR14_CH1, TMR1_CH1N, TMR17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7
PC4	24	-	-	-	I/O	TTa	-	EVENTOUT	ADC_IN14
PC5	25	-	-	-	I/O	TTa	-	TSC_G3_IO1	ADC_IN15
PB0	26	18	14	14	I/O	TTa	-	TMR3_CH3, TMR1_CH2N, TSC_G3_IO2, EVENTOUT	ADC_IN8
PB1	27	19	15	15	I/O	TTa	-	TMR3_CH4, TMR14_CH1, TMR1_CH3N, TSC_G3_IO3	ADC_IN9
PB2	28	20	-	16	I/O	FT	-	TSC_G3_IO4	-
PB10	29	21	-	-	I/O	FT	-	I2C2_SCL, CEC, TMR2_CH3, TSC_SYNC	-
PB11	30	22	-	-	I/O	FT	-	I2C2_SDA, TMR2_CH4, TSC_G6_IO1, EVENTOUT	-
V_{SS}	31	23	16	0	S	-	-	Ground	
V_{DD}	32	24	17	17	S	-	-	Digital power supply	
PB12	33	25	-	-	I/O	FT	-	SPI2_NSS, TMR1_BKIN, TSC_G6_IO2, EVENTOUT	-
PB13	34	26	-	-	I/O	FT	-	SPI2_SCK, TMR1_CH1N TSC_G6_IO3	-
PB14	35	27	-	-	I/O	FT	-	SPI2_MISO, TMR1_CH2N, TMR15_CH1, TSC_G6_IO4	-
PB15	36	28	-	-	I/O	FT	-	SPI2_MOSI, TMR1_CH3N, TMR15_CH1N, TMR15_CH2	RTC_REFIN
PC6	37	-	-	-	I/O	FT	-	TMR3_CH1	-
PC7	38	-	-	-	I/O	FT	-	TMR3_CH2	-

Pin name (Function after reset)	Pin code				Pin Type	I/O Structure	Note	Pin function	
	LQFP 64	LQFP48/QFN48	LQFP 32	QFN 32				Multiplexing function	Additional function
PC8	39	-	-	-	I/O	FT	-	TMR3_CH3	-
PC9	40	-	-	-	I/O	FT	-	TMR3_CH4	-
PA8	41	29	18	18	I/O	FT	-	USART1_CK, TMR1_CH1, EVENTOUT, MCO	-
PA9	42	30	19	19	I/O	FT	-	USART1_TX, TMR1_CH2, TMR15_BKIN, TSC_G4_IO1	-
PA10	43	31	20	20	I/O	FT	-	USART1_RX, TMR1_CH3, TMR17_BKIN, TSC_G4_IO2	-
PA11	44	32	21	21	I/O	FT	-	USART1_CTS, TMR1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT	-
PA12	45	33	22	22	I/O	FT	-	USART1_RTS, TMR1_ETR, COMP2_OUT, TSC_G4_IO4, EVENTOUT	-
PA13 (SWDIO)	46	34	23	23	I/O	FT	(2)	IR_OUT, SWDIO	-
PF6	47	35	-	-	I/O	FT	-	I2C2_SCL	-
PF7	48	36	-	-	I/O	FT	-	I2C2_SDA	-
PA14 (SWCLK)	49	37	24	24	I/O	FT	(2)	USART2_TX, SWCLK	-
PA15	50	38	25	25	I/O	FT	-	SPI1_NSS, I2S1_WS, USART2_RX, TMR2_CH1_ETR, EVENTOUT	-
PC10	51	-	-	-	I/O	FT	-	-	-
PC11	52	-	-	-	I/O	FT	-	-	-
PC12	53	-	-	-	I/O	FT	-	-	-
PD2	54	-	-	-	I/O	FT	-	TMR3_ETR	-
PB3	55	39	26	26	I/O	FT	-	SPI1_SCK, I2S1_CK, TMR2_CH2, TSC_G5_IO1, EVENTOUT	-
PB4	56	40	27	27	I/O	FT	-	SPI1_MISO, I2S1_MCK, TMR3_CH1, TSC_G5_IO2, EVENTOUT	-
PB5	57	41	28	28	I/O	FT	-	SPI1_MOSI, I2S1_SD, I2C1_SMBA, TMR16_BKIN, TMR3_CH2	

Pin name (Function after reset)	Pin code				Pin Type	I/O Structure	Note	Pin function	
	LQFP 64	LQFP48/QFN48	LQFP 32	QFN 32				Multiplexing function	Additional function
PB6	58	42	29	29	I/O	FTf	-	I2C1_SCL, USART1_TX, TMR16_CH1N, TSC_G5_IO3	-
PB7	59	43	30	30	I/O	FTf	-	I2C1_SDA, USART1_RX, TMR17_CH1N, TSC_G5_IO4	-
BOOT0	60	44	31	31	I	B	-	Startup selection	
PB8	61	45	-	32	I/O	FTf	-	I2C1_SCL, CEC, TMR16_CH1, TSC_SYNC	-
PB9	62	46	-	-	I/O	FTf	-	I2C1_SDA, IR_OUT, TMR17_CH1, EVENTOUT	-
V_{SS}	63	47/0	32	0	S	-	-	Ground	
V_{DD}	64	48	1	1	S	-	-	Digital power supply	

Note:

(1) PC13, PC14 and PC15 are powered through power switch. Since the switch only sinks limited current (3mA), the use of GPIO from PC13 to PC15 in output mode is limited: the speed shall not exceed 2MHz when the heavy load is 30pF; not used for current source (eg.driving LED).

(2) After reset, these pins are configured as SWDIO and SWCLK multiplexing functions, and the internal pull-up of SWDIO pin and the internal pull-down of SWCLK pin are activated.

Table 4 Port A Multiplex Function Configuration

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	USART2_CTS	TMR2_CH1_ETR	TSC_G1_IO1	-	-	-	COMP1_OUT
PA1	EVENTOUT	USART2_RTS	TMR2_CH2	TSC_G1_IO2	-	-	-	-
PA2	TMR15_CH1	USART2_TX	TMR2_CH3	TSC_G1_IO3	-	-	-	COMP2_OUT
PA3	TMR15_CH2	USART2_RX	TMR2_CH4	TSC_G1_IO4	-	-	-	-
PA4	SPI1_NSS, I2S1_WS	USART2_CK	-	TSC_G2_IO1	TMR14_CH1	-	-	-
PA5	SPI1_SCK, I2S1_CK	CEC	TMR2_CH1_ETR	TSC_G2_IO2	-	-	-	-
PA6	SPI1_MISO, I2S1_MCK	TMR3_CH1	TMR1_BKIN	TSC_G2_IO3	-	TMR16_CH1	EVENTOUT	COMP1_OUT
PA7	SPI1_MOSI, I2S1_SD	TMR3_CH2	TMR1_CH1N	TSC_G2_IO4	TMR14_CH1	TMR17_CH1	EVENTOUT	COMP2_OUT
PA8	MCO	USART1_CK	TMR1_CH1	EVENTOUT	-	-	-	-
PA9	TMR15_BKIN	USART1_TX	TMR1_CH2	TSC_G4_IO1	-	-	-	-
PA10	TMR17_BKIN	USART1_RX	TMR1_CH3	TSC_G4_IO2		-	-	-
PA11	EVENTOUT	USART1_CTS	TMR1_CH4	TSC_G4_IO3	-	-	-	COMP1_OUT
PA12	EVENTOUT	USART1_RTS	TMR1_ETR	TSC_G4_IO4	-	-	-	COMP2_OUT
PA13	SWDIO	IR_OUT	-	-	-	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-	-
PA15	SPI1_NSS, I2S1_WS	USART2_RX	TMR2_CH1_ETR	EVENTOUT	-	-	-	-

Table 5 Port B Multiplexing Function Configuration

Pin name	AF0	AF1	AF2	AF3
PB0	EVENTOUT	TMR3_CH3	TMR1_CH2N	TSC_G3_IO2
PB1	TMR14_CH1	TMR3_CH4	TMR1_CH3N	TSC_G3_IO3
PB2	-	-	-	TSC_G3_IO4
PB3	SPI1_SCK,I2S1_CK	EVENTOUT	TMR2_CH2	TSC_G5_IO1
PB4	SPI1_MISO,I2S1_MCK	TMR3_CH1	EVENTOUT	TSC_G5_IO2
PB5	SPI1_MOSI,I2S1_SD	TMR3_CH2	TMR16_BKIN	I2C1_SMBA
PB6	USART1_TX	I2C1_SCL	TMR16_CH1N	TSC_G5_IO3
PB7	USART1_RX	I2C1_SDA	TMR17_CH1N	TSC_G5_IO4
PB8	CEC	I2C1_SCL	TMR16_CH1	TSC_SYNC
PB9	IR_OUT	I2C1_SDA	TMR17_CH1	EVENTOUT
PB10	CEC	I2C2_SCL	TMR2_CH3	TSC_SYNC-
PB11	EVENTOUT	I2C2_SDA	TMR2_CH4	TSC_G6_IO1
PB12	SPI2_NSS	EVENTOUT	TMR1_BKIN	TSC_G6_IO2
PB13	SPI2_SCK	-	TMR1_CH1N	TSC_G6_IO3

Pin name	AF0	AF1	AF2	AF3
PB14	SPI2_MISO	TMR15_CH1	TMR1_CH2N	TSC_G6_IO4
PB15	SPI2_MOSI	TMR15_CH2	TMR1_CH3N	TMR15_CH1N

4 Functional description

APM32F051x6x8 series chips are Arm® Cortex®-M0+core based 32-bit high-performance MCU with a maximum operating frequency of 48MHz. Built in high-speed memory (up to 64K-byte flash and 8K-bytes SRAM), chip pins multiplexes a large number of enhanced peripherals and I/Os. All chips provide standard communication interfaces: I2C interface, USART interface, SPI interface ad HDMI CEC.

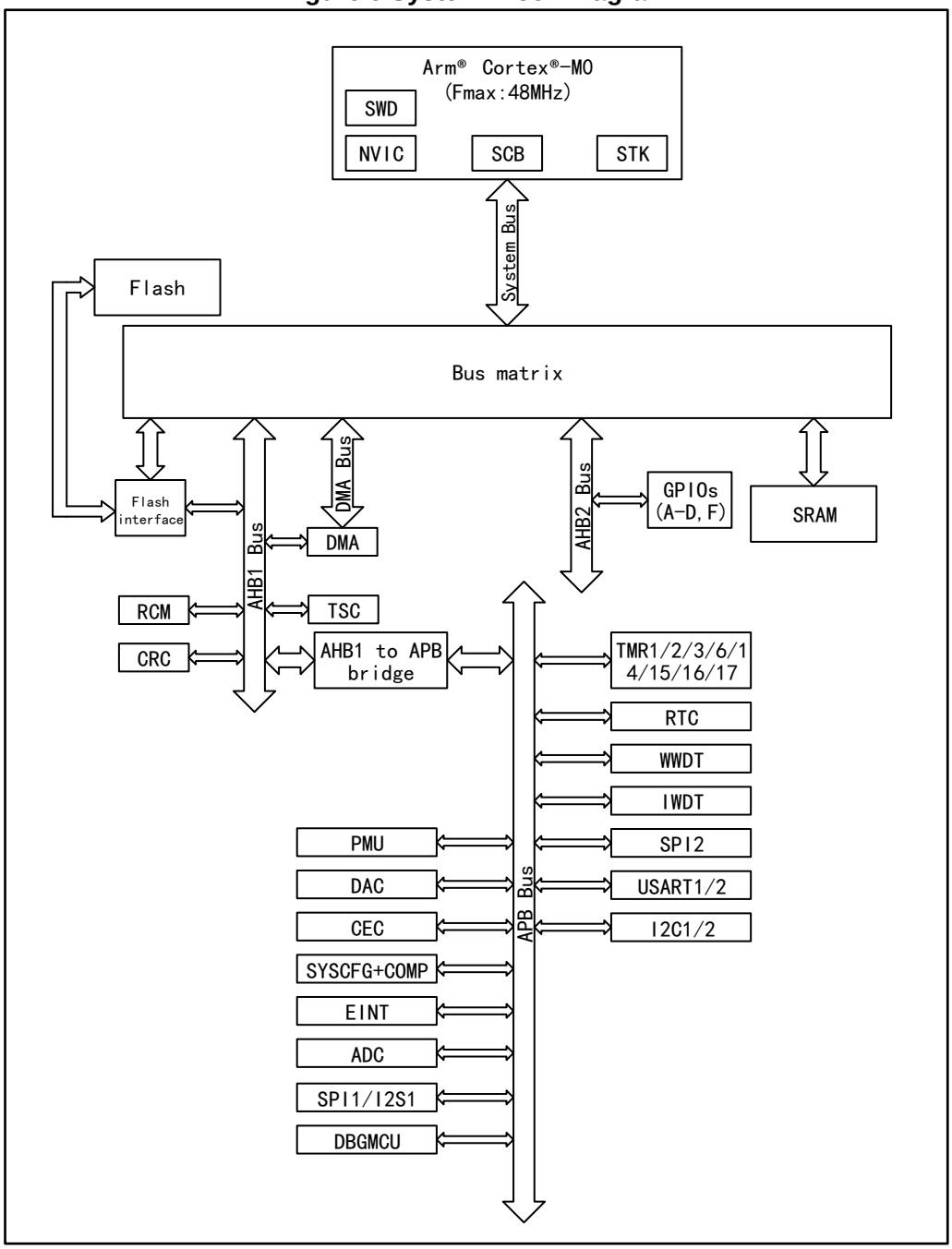
The ambient temperature range of APM32F051x6x8 MCU is -40~+85℃ and -40℃~+105℃, and the voltage range is 2.0-3.6V. Many power saving modes ensure the requirements of low power consumption application.

APM32F051x6x8 MCU includes various different packaging forms, and different packaging forms make the device peripheral configuration not exactly the same.

For information about the Arm® Cortex®-M0+ core, please refer to the Arm® Cortex®-M0+ technical reference manual, which can be downloaded from Arm's website.

4.1 System Block Diagram

Figure 6 System Block Diagram



4.2 Core

Arm® Cortex®-M0+ core is the latest-generation embeded Arm core. It is a low-cost platform, APM32 is developed based on this platform, and is optimized on the system power consumption, at the same time, APM32 provides excellent computing performance and advanced system interrupt response.

APM32F0xx series is based on embedded Arm core, so it is compatible with all Arm tools and software.

4.3 Memory

See the table below for memory details:

Table 6 Memory Description

Memory	Maximum bytes	Function
Main memory	64KB	Store programs and data
SRAM	8KB	Store temporary data
System memory area	3KB	BootLoader, product ID, and product main memory area information
Option byte	16bytes	Write protection of main memory

4.4 Memory mapping

Table 7 APM32051x6x8 Storage Mapping Table

Region	Start address	Name
Code	0x0000 0000	Code mapping area
Code	0x0001 0000	Reserved
Code	0x0800 0000	Main memory area
Code	0x0801 0000	Reserved
Code	0x1FFF EC00	System memory area
Code	0x1FFF F800	Option byte
Code	0x1FFF FC00	Reserved
SRAM	0x2000 0000	SRAM
—	0x2000 2000	Reserved
APB bus	0x4000 0000	TMR2
APB bus	0x4000 0400	TMR3
APB bus	0x4000 0800	Reserved
APB bus	0x4000 1000	TMR6
APB bus	0x4000 1800	Reserved
APB bus	0x4000 2000	TMR14
APB bus	0x4000 2400	Reserved
APB bus	0x4000 2800	RTC
APB bus	0x4000 2C00	WWDT
APB bus	0x4000 3000	IWDT
APB bus	0x4000 3400	Reserved
APB bus	0x4000 3800	SPI2

Region	Start address	Name
APB bus	0x4000 3C00	Reserved
APB bus	0x4000 4400	USART2
APB bus	0x4000 5000	Reserved
APB bus	0x4000 5400	I2C1
APB bus	0x4000 5800	I2C2
APB bus	0x4000 6800	Reserved
APB bus	0x4000 7000	PMU
APB bus	0x4000 7400	DAC
APB bus	0x4000 7800	CEC
APB bus	0x4000 7C00	Reserved
—	0x4000 8000	Reserved
APB bus	0x4001 0000	SYSCFG+COMP
APB bus	0x4001 0400	EINT
APB bus	0x4001 0800	Reserved
APB bus	0x4001 2400	ADC
APB bus	0x4001 2800	Reserved
APB bus	0x4001 2C00	TMR1
APB bus	0x4001 3000	SPI1/I2S1
APB bus	0x4001 3400	Reserved
APB bus	0x4001 3800	USART1
APB bus	0x4001 3C00	Reserved
APB bus	0x4001 4000	TMR15
APB bus	0x4001 4400	TMR16
APB bus	0x4001 4800	TMR17
APB bus	0x4001 4C00	Reserved
APB bus	0x4001 5800	DBGMCU
APB bus	0x4001 5C00	Reserved
—	0x4001 8000	Reserved
AHB1 bus	0x4002 0000	DMA
AHB1 bus	0x4002 0800	Reserved
AHB1 bus	0x4002 1000	RCM
AHB1 bus	0x4002 1400	Reserved
AHB1 bus	0x4002 2000	Flash interface
AHB1 bus	0x4002 2400	Reserved
AHB1 bus	0x4002 3000	CRC
AHB1 bus	0x4002 3400	Reserved
AHB1 bus	0x4002 4000	TSC
—	0x4002 4400	Reserved
AHB2 bus	0x4800 0000	GPIOA

Region	Start address	Name
AHB2 bus	0x4800 0400	GPIOB
AHB2 bus	0x4800 0800	GPIOC
AHB2 bus	0x4800 0C00	GPIOD
—	0x4800 1000	Reserved
AHB2 bus	0x4800 1400	GPIOF
—	0x4800 1800	Reserved
Core	0xE000 E010	STK
Core	0xE000 E100	NVIC
Core	0xE000 ED00	SCB
—	0xE010 0000	Reserved

4.5 Power Management

4.5.1 Power Supply Scheme

Table 8 Power Supply Scheme

Name	Voltage range	Instruction
V_{DD}=V_{DDIO1}	2.0~3.6V	V_{DD} powers IO interface directly, and powers core circuit through voltage regulator
V_{DDA}	V_{DD}~3.6V	The V_{DDA} supplies power to the ADC, DAC, reset module, RC oscillator and PLL. The voltage level of V_{DDA} must always be greater than or equal to the voltage level of V_{DD}, which should be given priority
V_{BAT}	1.65-3.6V	When V_{DD} is powered off, RTC, external 32KHz oscillator and backup register are supplied through V_{BAT} pin.

Note: See the power supply scheme for more detailed information about how to connect the power pins.

4.5.2 Voltage regulator

The voltage regulator has three modes, and can adjust the working mode of MCU so as to reduce power consumption. See the table below for details of the three modes.

Table 9 Working Modes of Voltage Regulator

Name	Instruction
Master mode (MR)	Used in normal working mode.
Low-power mode (LPR)	Used in stop mode when you need to reduce the power.
Power-down mode	Used in power standby mode, when the voltage regulator has high impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.5.3 Power Supply Monitor

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value $V_{POR/PDR}$, the system will keep the reset state without connecting the external reset circuit.

The product has a built-in programmable voltage regulator (PVD) that can monitor V_{DD} and compare it with V_{PVD} threshold. When V_{DD} is outside the V_{PVD} threshold range and the interrupt is enabled, the MCU can be set to a safe state through the interrupt service program.

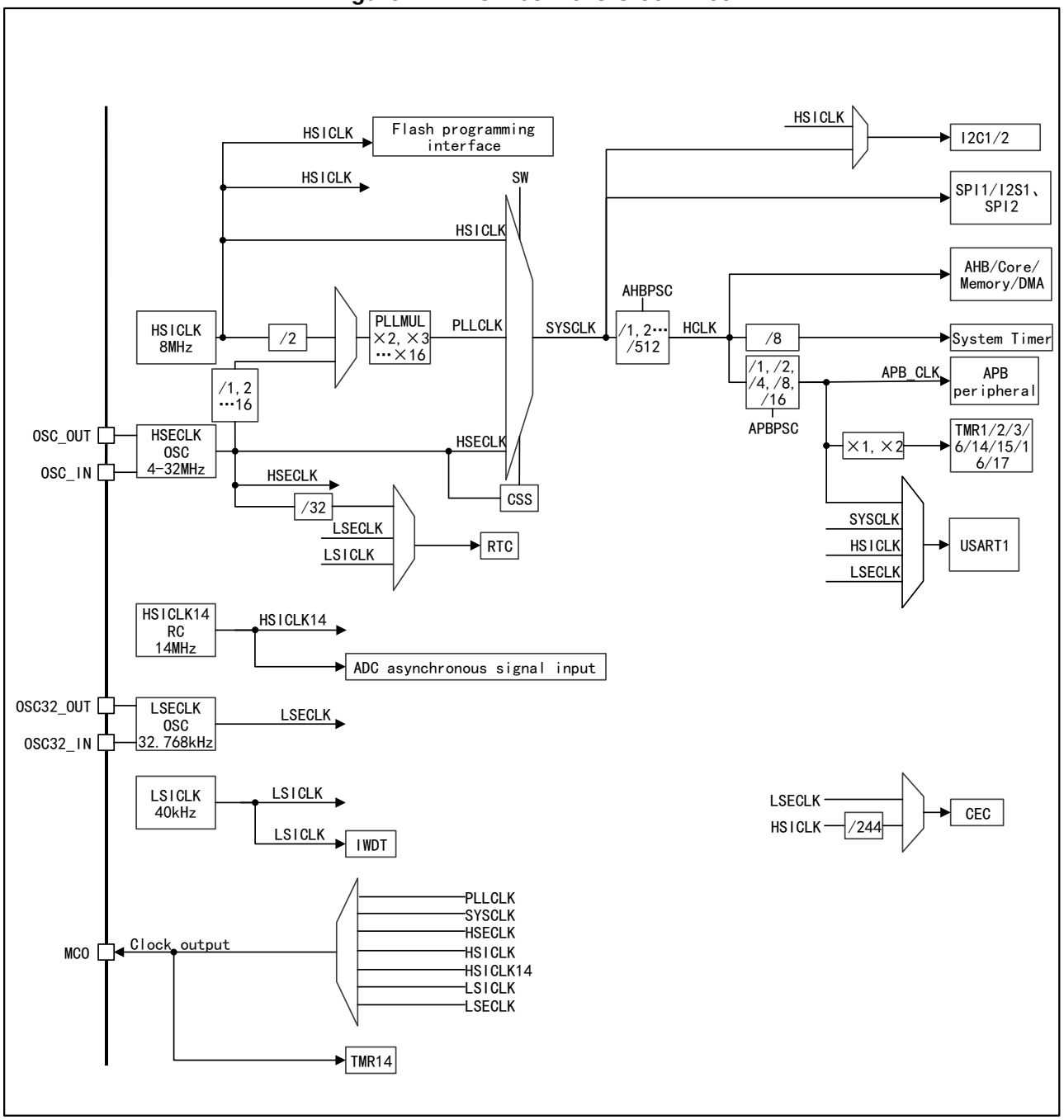
Table 10 Low-power Mode

Mode type	Instruction
Sleep mode	The CPU stops working, all peripherals are working, and interrupts/events can wake up the CPU.
Stop mode	Under the condition that SRAM and register data are not lost, the stop mode can achieve the lowest power consumption; The clock of the internal 1.5V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be prohibited, and the voltage regulator can be configured in normal mode or low power mode; Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, PVD output, RTC, I2C1, USART1, USART2, analog comparator and CEC.
Standby mode	The power consumption in this mode is the lowest; Internal voltage regulator is turned off, all 1.5V power supply modules are powered off, HSECLK crystal resonator, HSICLK and PLL clocks are turned off, SRAM and register data disappear, RTC area and backup register contents remain, and standby circuit still works; The external reset signal on NRST, IWDT reset, rising edge on WKUP pin or RTC event will wake MCU out of standby mode.

Note: RTC, IWDT and corresponding clocks still work normally in stop or standby mode.

4.6 Clock tree

Figure 7 APM32F051x6x8 Clock Tree



4.7 Clocks and startup

Users can use 4~32MHz external high-speed clock with "failure monitoring" function through configuration. When the system clock does not detect that the external clock is configured, the system will automatically switch to the internal RC oscillator.

4.8 Real-time clock (RTC)

A built-in RTC with LSECLK signal input pins (OSC32_IN, OSC32_OUT), 2 TAMP input signal detection pins (RTC_TAMP1/2), one reference clock input signal (RTC_REFIN), one output timestamp event output pin (RTC_TS), and one signal output pin RTC_OUT (it can be configured as calibration signal output or alarm clock signal output).

The external crystal oscillator, resonator or oscillator, LSICLK and HSECLK/32 with external frequency of 32.768kHz can be selected as the clock source.

With calendar function, it can display sub-seconds, seconds, minutes, hours (12 or 24 hours format), weeks, dates, months and years. It supports alarm clock function, and can output the alarm clock signal for external use, and wake up from low power consumption mode. It can receive signals to wake up from low power consumption mode. In terms of accuracy, it supports daylight saving time compensation, month angel compensation and leap year days compensation. In terms of precision, the error caused by crystal oscillator can be repaired by RTC digital calibration function, and the accuracy of calendar can be improved by using a more accurate second source clock (50 or 60Hz).

4.9 Startup mode

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from user Flash
- Startup from system memory
- Startup from embedded SRAM

Users can use USART to reprogram user Flash (ISP) when startup from system memory.

4.10 CRC computing unit

A CRC (Cyclic Redundancy Check) calculation unit obtains a CRC code through a generator polynomial algorithm.

4.11 Interrupt controller

4.11.1 Nested Vector Interrupt Controller (NVIC)

The APM32F051x6x8 product has a nested vector interrupt controller, and NVIC can handle up to 32 maskable interrupt channels (excluding 16 interrupt lines of Arm® Cortex®-Mx) and 4 priorities.

Nested Vector Interrupt Controller (NVIC) has a tightly coupled NVIC interface, which directly transmits the interrupt vector entry address to the kernel, so as to achieve low-delay interrupt response processing. In addition, it can give priority to late arriving higher priority interrupts and supports tail links and the processor state is saved automatically.

4.11.2 External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 24 edge detectors that generate event/interrupt requests. Its trigger events (rising edge or falling edge or double edge) can be independently configured or shielded; there is a register that holds the status of all interrupt requests. Up to 55 general-purpose I/Os can be connected to 16 external interrupt lines. EINT can detect pulses whose width is smaller than the internal clock cycle.

4.12 DMA

A built-in DMA supports 5 DMA channels, each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI1/2, USART1/2, I2C1/2, TMR1, TMR2, TMR3, TMR6, TMR15, TMR16 and TMR17. Four levels of DMA channel priority can be configured, and data transmission of "Memory → Memory, Memory → Peripheral, Peripheral → Memory" can be supported (memory includes Flash and SRAM).

4.13 Timer

The APM32F051x6x8 product includes up to five general-purpose timers, a basic timer and an advanced control timer.

Table 11 Advanced Control Timer

Timer type	Advanced control timer
Timer	TMR1
Counter resolution	16 bits
Counter type	Up, down, up/down
Prescaler coefficient	Any integer between 1 and 65536
DMA request generation	Yes
Capture/Comparison channel	4
Complementary outputs	Yes
Functional Description	It has complementary PWM output with dead band insertion, and can also be regarded as a complete general-purpose timer. It has 4 independent channels, used for input capture/output comparison, PWM or single-pulse mode output. When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, the timer can be frozen. Synchronization or event chaining function provided.

Table 12 Basic Timer

Timer type	Basic timer
Timer	TMR6
Counter resolution	16 bits
Counter type	Up
Prescaler coefficient	Any integer between 1 and 65536
DMA request generation	Yes
Capture/Comparison channel	0
Complementary outputs	-
Functional Description	It is mainly used for generation of DAC trigger, and can also be used as a general-purpose 16-bit timebase clock

Table 13 General-purpose Timer

Timer type	General-purpose timer					
Timer	TMR2	TMR3	TMR14	TMR15	TMR16	TMR17

Timer type	General-purpose timer				
Counter resolution	32 bits	16 bits	16 bits	16 bits	16 bits
Counter type	Up, down Up/Down		Up	Up	Up
Prescaler	Any integer between 1 and 65536		Any integer between 1 and 65536	Any integer between 1 and 65536	Any integer between 1 and 65536
DMA request generation	Yes		None	Yes	Yes
Capture/comparison channels	4		1	2	1
Functional Description	It has complementary output function with dead zone generation and independent DMA request generation. These two timers can work together, They have 4 independent channels, used for input capture/output comparison, PWM or single-pulse mode output. Up to 12 input capture, output comparison or PWM channels can be provided in the largest package configuration.		Single channel and PWM function for input capture/output comparison.	It has complementary output function with dead zone generation and independent DMA request generation. These three timers can work together, and TMR15 operates with TMR1 through link function, which can realize synchronization or event link function. TMR15 has two independent channels, while TMR16 and TMR17 only have one.	

Table 14 Independent Watchdog and Window Watchdog Timer Comparison

Name	Counter Resolution	Counter type	Prescaler factor	Functional Description
Independent watchdog timer (IWDT)	12-bit	Down	between 1~256 Any integer	The clock is provided by an internally independent RC oscillator of 40KHz, which is independent of the master clock, so it can run in stop and standby modes. The whole system can be reset in case of problems. It can provide timeout management for applications. It can be configured as a software or hardware startup watchdog. In debug mode, the counter can be paused for convenience of debugging.
Window watchdog （WWDT）	7-bit	Down	-	Can be set for free running. The whole system can be reset in case of problems. Driven by the master clock, it has early interrupt warning function. Timers in debug mode can be frozen.

4.14 System tick timer

System tick timer is a standard 24-bit down counter with automatic reloading function. When the counter is 0, it can generate a maskable system interrupt and can program the clock source (HCLK or HCLK/8).

4.15 Communication interface

4.15.1 I2C bus

I2C1/2 can work in master mode and slave mode, and supports 7-bit and 10-bit addressing modes. I2C1/2 supports standard mode (up to 100kbit/s) or fast mode (up to 400kbit/s). In addition, I2C1 has built-in programmable analog and digital noise filters, and also supports ultra-fast mode (up to 1 Mbit/s).

In addition, I2C1 also provides hardware support for SMBUS2.0 and PMBUS1.1: master notification protocol, hardware CRC (PEC) generation / verification, ARP function, timeout verification and alarm protocol management.

4.15.2 Universal synchronous/asynchronous transmitter receiver (USART)

Up to 2 universal synchronous/asynchronous transmitter receivers are embedded in the chip, and the communication rate can support 6Mbit/s at most. All USART interfaces can be provided by DMA controller, and it supports single-line half duplex mode, modem hardware control, multiprocessor communication and synchronization mode. In addition, USART1 also supports wake-up receiving timeout interrupt, MODBUS communication and baud rate automatic detection in smart card mode, infrared control mode, LIN mode, dual clock domain and stop mode.

4.15.3 Serial peripheral interface SPI/I2S bus

Two SPI interfaces are embedded, which enables the chip to communicate with external devices in half/full duplex serial mode. The interface can be configured as master mode or slave mode. Eight master mode frequencies can be generated by a 3-bit prescaler, with 4~16 bits per frame and a communication rate of 18 Mbit/s. Both interfaces support hardware cyclic redundancy check calculation, receive/transmit FIFO, NSS pulse mode and TI mode. Besides, SPI1 also supports I2S.

4.16 General-purpose input and output interface (GPIO)

The working mode of GPIO can be configured as general input, general output, multiplexing function and analog input/output; the general input can be configured as floating input, pull-up input and pull-down input; the general output can be configured as push-pull output and open-drain output; the multiplexing function can be used for digital peripherals; and the analog input and output can be used for analog peripherals and low-power mode; the enable and disable pull-up/pull-down resistor can be configured; the speed of 2MHz, 10MHz and 50MHz can be configured; the higher the speed is, the greater the power and the noise will be.

4.17 Analog peripherals

4.17.1 ADC (analog/digital converter)

The 12-bit A/D converter has up to 16 external channels and 3 internal channels, which can perform single or scanning conversion.

The analog watchdog function can monitor multiple channels very accurately, and when the monitored signal exceeds the threshold value, an interrupt will be generated.

ADC supports DMA function.

4.17.2 Internal reference voltage (V_{REFINT})

The internal reference voltage (V_{REFINT}) provides a stable (band gap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel, which is accessed in read-only mode.

Table 15 Internal Reference Voltage Calibration Value

Calibration Value Name	Description	Memory Address
VREFINT_CAL	Original data collected at 30°C(± 5 °C) and V_{DDA} = 3.3V (10mV)	0x1FFF F7BA - 0x1FFF F7BB

4.17.3 V_{BAT} Monitor

The built-in V_{BAT} monitor is internally connected to a 2-divider bridge, and $V_{BAT}/2$ is connected to ADC_IN18 channel, which can be obtained through ADC.

4.17.4 DAC (digital/analog converter)

There is one built-in 12-bit DAC. The DAC corresponds to an output channel, which can be configured as 12-bit mode of left or right data alignment, supports synchronous update function and DMA function and external signal trigger mode.

4.17.5 Comparator (COMP)

Two built-in fast rail-to-rail comparators, the internal/external reference voltage, hysteresis, speed and support are programmable, and the output polarity support is configurable. The reference voltage can be selected from external I/O, DAC output pin, internal reference voltage (VREFINT), and 1/4 or 1/2 or 3/4 of the internal reference voltage, which can generate interrupts, and support MCU entering sleep and stop modes by external interrupts.

4.17.6 Touch sensor controller (TSC)

Built-in touch sensing controller can detect the change of capacitance, which can be applied to touch keys. When a finger touches a key, capacitance will be introduced, which will cause the capacitance change, so as to judge whether there is an eye-catching key. The touch sensing is compatible with slider, touch key, linear and rotary.

Up to 24 GPIOs support capacitance sensor function, which are divided into 6 groups. In practical application, each sampling capacitor occupies one GPIO port, so up to 18 capacitance sensor channels are supported. See the table below for specific pin distribution.

Table 16 Applicable Pin Distribution of Touch Sensors

Group No.	Capacitance Sensor Signal Name	Pin name
G1	TSC_G1_IO1	PA0
G1	TSC_G1_IO2	PA1
G1	TSC_G1_IO3	PA2
G1	TSC_G1_IO4	PA3
—		
G2	TSC_G2_IO1	PA4
G2	TSC_G2_IO2	PA5
G2	TSC_G2_IO3	PA6
G2	TSC_G2_IO4	PA7
—		
G3	TSC_G3_IO1	PC5
G3	TSC_G3_IO2	PB0
G3	TSC_G3_IO3	PB1
G3	TSC_G3_IO4	PB2
—		
G4	TSC_G4_IO1	PA9
G4	TSC_G4_IO2	PA10
G4	TSC_G4_IO3	PA11
G4	TSC_G4_IO4	PA12
—		
G5	TSC_G5_IO1	PB3
G5	TSC_G5_IO2	PB4
G5	TSC_G5_IO3	PB6
G5	TSC_G5_IO4	PB7
—		
G6	TSC_G6_IO1	PB11
G6	TSC_G6_IO2	PB12
G6	TSC_G6_IO3	PB13
G6	TSC_G6_IO4	PB14

Table 17 Number of Touch Sensor Channels Supported by Each Model in Practical Application

Group No.	Number of Channels for Each Group of Capacitance Sensors			
	APM32F051Rx	APM32F051Cx	APM32F051KxT (LQFP32)	APM32F051KxU (QFN32)
G1	3	3	3	3
G2	3	3	3	3
G3	3	2	1	2
G4	3	3	3	3
G5	3	3	3	3
G6	3	3	0	0
Total Number of Capacitance Sensor Channels	18	17	13	14

4.18 Serial wire debug port (SW-DP)

The product provides Arm SW-DP interface, through which MCU can be connected with serial line debugging tool.

5 Electrical characteristics

5.1 Test condition

All voltage parameters (unless otherwise specified) refer to V_{SS}.

5.1.1 Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at T_A=25℃. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; On the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values.

5.1.2 Typical values

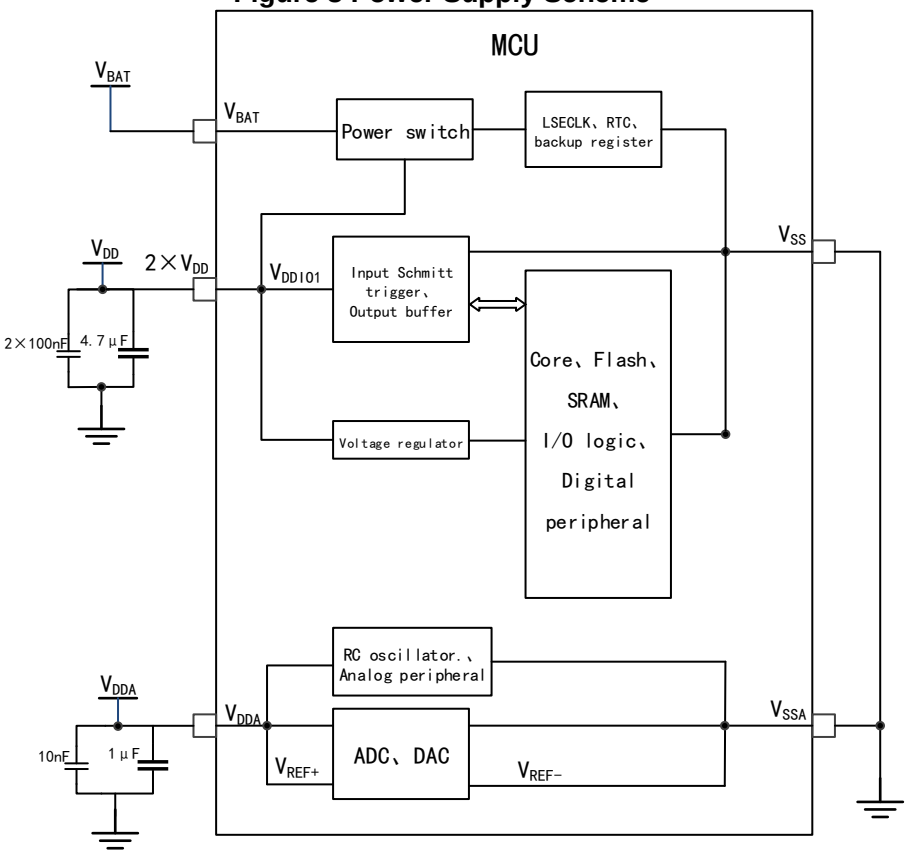
Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}= V_{DDA}=V_{BAT}=3.3V; these data are for design guidance only.

5.1.3 Typical curve

Unless otherwise specified, typical curves will not be tested on the production line, and will only be used for design guidance.

5.1.4 Power supply scheme

Figure 8 Power Supply Scheme



5.1.5 Load capacitance

Figure 9 Load conditions when measuring pin parameters

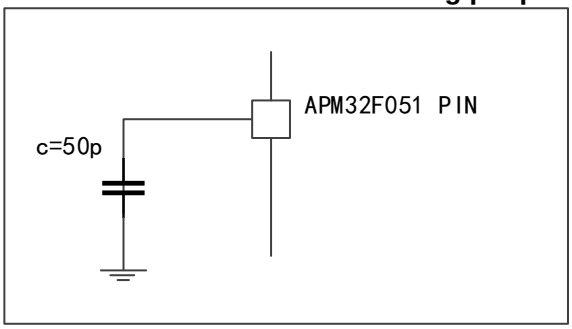


Figure 10 Pin Input Voltage Measurement Scheme

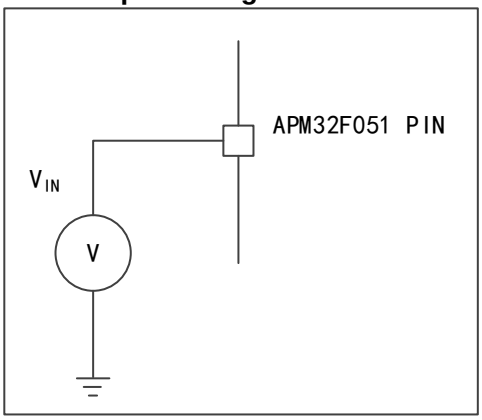
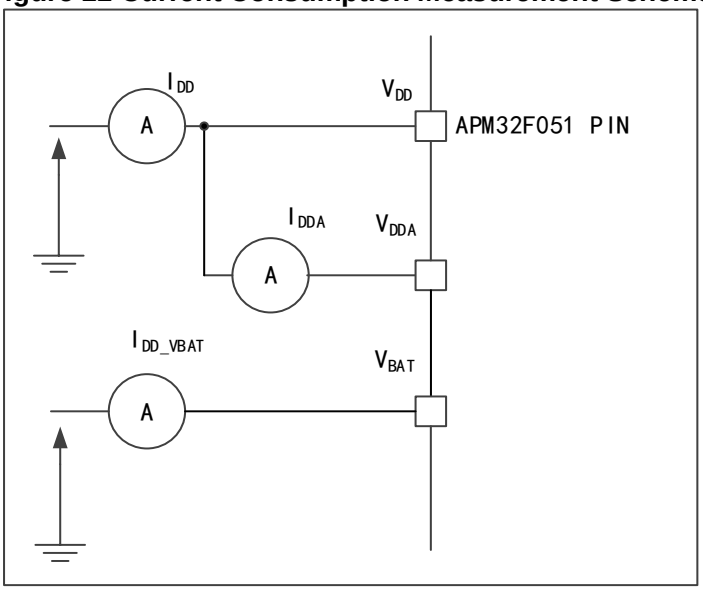


Figure 11 Current Consumption Measurement Scheme



5.2 Absolute maximum ratings

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.2.1 Maximum rated voltage characteristics

Table 18 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD}-V_{SS}	External main supply voltage (V_{DD}) (1)	-0.3	4.0	V
V_{DDA}-V_{SS}	External analog supply voltage (V_{DDA})	-0.3	4.0	
| V_{DD}-V_{DDA} |	Voltage difference allowed by V_{DD}>V_{DDA}	-	0.3	
V_{BAT}-V_{SS}	External backup supply voltge (V_{BAT})	-0.3	4.0	
V_{IN}	Input voltage on FT and FTf pins	V_{SS}-0.3	V_{DD}+4.0(2)	
	Input voltage on TTa pin	V_{SS}-0.3	4.0	
	BOOT0	0	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS}-0.3	4.0	
|ΔV_{DDx}|	Voltage difference between different power supply pins	-	50	mV
|V_{SSx}-V_{SS}|	Voltage difference between different grounding pins	-	50	

Note:

(1) V_{DD}, V_{DDA} and V_{SS}, and V_{SSA} pins must always be connected to external power supply, and V_{BAT} can be connected according to actual application.

(2) If IO is configured as pull-up or pull-down input, the maximum input voltage is 4V.

5.2.2 Maximum Rated Current Features

Table 19 Maximum Rated Current Features

Symbol	Description	Maximum	Unit
ΣI_{VDD}	Total current into sum of all V_{DD} power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	-120	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source) (1)	100	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
$I_{INJ(PIN)}$ (3)	Injected current onB,FT and FTf pins	-5/+0(4)	
	Injected current on TC and RST pins	±5	
	Injected current on TTa pins(5)	±5	
$\Sigma I_{INJ(PIN)}$(2)	Total injected current (sum of all I/O and control pins)(6)	±25	

Note:

(1) All power (V_{DD}，V_{DDA}) and ground (V_{SS}，V_{SSA}) pins must always be connected to a power

supply within the external allowable range.

(2) If V_{IN} does not exceed the maximum value, $I_{INJ(PIN)}$ will not exceed its limit. If VIN exceeds the maximum value, $I_{INJ(PIN)}$ must be externally limited to not exceed its maximum value. When $V_{IN} > V_{DD}$, there is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current.

(3) Reverse injection current can interfere with the analog performance of the ADC.

(4) When several I/O ports have injection current at the same Time, the maximum value of $\Sigma I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current. These results are based on the calculation of the maximum value of $\Sigma I_{INJ(PIN)}$ on the four I/O port pins of the device.

(5) On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device.

(6) When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.2.3 Maximum electrostatic characteristics

Table 20 Electrostatic Discharge (ESD)

Symbol	Parameter	Conditions	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=+25℃	4500	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A=+25℃	2000	

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.2.4 Static latch-up

Table 21 Static Latch-up

Symbol	Parameter	Conditions	Type
LU	Class of static latch-up	T_A=+25℃/105℃	class ⅡA

5.2.5 Maximum temperature characteristics

Table 22 Temperature Characteristics

Symbol	Description	Numerical Value	Unit
T_{STG}	Storage temperature range	–65~ +150	℃
T_J	Maximum junction temperature	150	℃

5.3 Test under general operating conditions

Table 23 General Operating Conditions

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	2	3.6	V

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
V_{DDA}	Analog partial operating voltage (When neither ADC nor DAC is used)	V_{DDA} must not be less than V_{DD}	V_{DD}	3.6	V
	Analog partial operating voltage (When ADC and DAC are used)		2.4	3.6	V
V_{BAT}	Standby supply voltage	-	1.65	3.6	V
V_{IN}	I/O input voltage	T_C and RSTI/O	-0.3	V_{DD}+0.3	V
		TTa I/O	-0.3	V_{DDA}+0.3	
		FT and FTf I/O	-0.3	5.5	
		BOOT0	0	5.5	

5.3.1 Power-on/power-down characteristics

Table 24 Power-on/power-down Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{VDD}	V_{DD} rise time rate	-	1	-	310000	μs/V
	V_{DD} fall time rate		1	-	310000	

5.3.2 Test of Embedded Reset and Power Control Block Characteristics

Table 25 Embedded Reset and Power Control Block Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
$V_{POR/PDR}$(1)	Power-on/power-down reset threshold	Falling edge (2)	-	1.87	-	V
		Rising edge	-	1.92	-	V
$V_{PDRhyst}$(3)	PDR hysteresis	-	-	50	-	mV
$T_{RSTTEMPO}$(3)	Reset duration	-	1.70	2.51	3.32	ms

Note:

(1) PDR detector monitors V_{DD} and V_{DDA} (if enabled in option byte), POR detector monitors V_{DD} only.

(2) Product characteristics are guaranteed by design to the minimum $V_{POR/PDR}$ value

(3) Guaranteed by design and not tested in production.

Table 26 Programmable Power Supply Voltage Detector Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{PVD}	Programmable power supply voltage detector voltage level selection	PLS[2:0]=000 (rising edge)	2.16	2.20	2.24	V
		PLS[2:0]=000 (falling edge)	2.06	2.10	2.14	V
		PLS[2:0]=001 (rising edge)	2.25	2.30	2.36	V
		PLS[2:0]=001 (falling edge)	2.14	2.20	2.25	V
		PLS[2:0]=010 (rising edge)	2.37	2.40	2.44	V
		PLS[2:0]=010 (falling edge)	2.26	2.30	2.33	V
		PLS[2:0]=011 (rising edge)	2.46	2.50	2.54	V
		PLS[2:0]=011 (falling edge)	2.36	2.40	2.43	V

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
		PLS[2:0]=100 (rising edge)	2.57	2.60	2.62	V
		PLS[2:0]=100 (falling edge)	2.46	2.50	2.51	V
		PLS[2:0]=101 (rising edge)	2.61	2.70	2.79	V
		PLS[2:0]=101 (falling edge)	2.52	2.60	2.68	V
		PLS[2:0]=110 (rising edge)	2.74	2.80	2.87	V
		PLS[2:0]=110 (falling edge)	2.62	2.70	2.76	V
		PLS[2:0]=111 (rising edge)	2.81	2.90	2.99	V
		PLS[2:0]=111 (falling edge)	2.71	2.80	2.89	V
$V_{PVDhyst}$	PVD hysteresis	-	-	100	-	mV

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.3.3 Test of Built-in Reference Voltage Characteristics

Table 27 Built-in Reference Voltage

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{REFINT}	Built-in Reference Voltage	-40℃ < T_A < +105℃	1.19	1.20	1.23	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10	μs
$T_{S\_vrefint}$	Sampling time of ADC when reading out internal reference voltage	-	4	-	-	μs
ΔV_{REFINT}	Built-in reference voltage extends to temperature range	V_{DDA}=3.3V	-	-	10	mV

5.3.4 Power consumption

Power consumption test environment

（1） The values are measured by executing Dhrystone 2.1, with the KeilV5 compilation environment and the L0 compilation optimization level.

（2） All I/O pins are configured as analog inputs and are connected to a static level of V_{DD} or V_{SS} (non-loaded).

（3） Unless otherwise specified, all peripherals are turned off.

（4） The relationship between Flash waiting cycle setting and f_{HCLK}:

- 0~24MHz: 0 waiting cycle;
- 24~48MHz: 1 waiting cycle.

（5） When it is greater than 24MHz, the instruction prefetch function is enabled (Note: this must be set before clock setting and bus frequency division).

（6） When the peripherals are enabled: f_{PCLK}=f_{HCLK}.

Table 28 Power Consumption in Run Mode when the Program is Executed in Flash

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}（μA）	I_{DD}(mA）	I_{DDA}(μA)	I_{DD}(mA)
Run mode	External clock (2), enabling all peripherals	48MHz	105.69	10.0	125.76	10.39
		24MHz	59.64	5.67	74.78	5.88
		8MHz	1.44	2.31	7.7	2.43
	External clock (2) , turning off all peripherals	48MHz	105.73	6.94	125.99	7.18
		24MHz	59.7	4.17	75.09	4.29
		8MHz	1.45	1.80	7.15	1.90
	Internal clock, enabling all peripherals	48MHz	161.22	9.6	187.84	10.04
		24MHz	115.39	5.24	137.09	5.45

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}（μA）	I_{DD}(mA）	I_{DDA}(μA)	I_{DD}(mA)
	Internal clock, turning off all peripherals	8MHz	57.97	1.88	72.8	1.97
		48MHz	161.54	6.51	187.58	6.82
		24MHz	115.50	3.66	136.98	3.85
		8MHz	58.0	1.33	72.45	1.40

Note:

(1) Data based on comprehensive evaluation will not be tested in production unless otherwise specified.

(2) The external clock is 8MHz. when f_{HCLK}>8MHz, PLL is started.

Table 29 Power Consumption in Run Mode when the Program is Executed in SRAM

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Run mode	External clock (2), enabling all peripherals	48MHz	105.73	7.48	125.63	7.75
		24MHz	59.67	4.08	74.76	4.30
		8MHz	1.44	1.8	7.20	1.88
	External clock (2) , turning off all peripherals	48MHz	105.78	4.40	125.98	4.60
		24MHz	59.71	2.54	74.96	2.69
		8MHz	1.45	1.27	7.11	1.35
	Internal clock, enabling all peripherals	48MHz	161.43	7.06	187.25	7.39
		24MHz	115.40	3.65	136.83	3.85
		8MHz	57.99	1.37	72.45	1.43
	Internal clock, turning off all peripherals	48MHz	161.62	3.94	187.61	4.14
		24MHz	115.49	2.07	137.02	2.23
		8MHz	58.04	0.79	72.4	0.86

Note:

(1) The data are obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz. when f_{HCLK}>8MHz, PLL is started.

Table 30 Power Consumption in Sleep Mode when the Program is Executed in SRAM or Flash

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Sleep mode	External clock (2), enabling all peripherals	48MHz	105.77	5.41	125.88	5.54
		24MHz	59.70	3.03	74.91	3.16
		8MHz	1.45	1.42	7.12	1.50
	External clock (2) , turning off all peripherals	48MHz	105.86	2.0	125.9	2.13
		24MHz	59.8	1.35	75.08	1.47
		8MHz	1.44	0.84	7.14	0.94
	Internal clock, enabling all peripherals	48MHz	161.55	4.93	187.25	5.14
		24MHz	115.48	2.60	136.87	2.72
		8MHz	58.0	0.99	72.41	1.05
	Internal clock, turning off all peripherals	48MHz	161.71	1.52	187.85	1.69
		24MHz	115.54	0.86	137.13	0.99
		8MHz	58.0	0.37	72.35	0.46

Note:

(1) The data are obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz. when f_{HCLK}>8MHz, PLL is started.

Table 31 Power Consumption in Stop Mode and Standby Mode

Parameter	Conditions		Typical values (T_A=25℃)				Maximum value (1) (T_A=105℃)	
			V_{DD}=2.4 V		V_{DD}= 3.3V		V_{DD}=3.6 V	
			I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)
Stop mode	V_{DDA} monitoring ON	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF	2.43	21.1	2.98	21.9	7.0	62.6
		Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF	2.43	6.47	2.98	7.42	7.0	44.9
Standby mode		Low-speed internal RC oscillator and independent watchdog ON	2.62	2.42	3.33	3.72	6.63	22.2
		Low-speed internal RC oscillator and independent watchdog OFF	2.28	1.96	2.83	3.08	6.11	21.5
Stop mode	V_{DDA} monitoring OFF	Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF	1.25	6.33	1.45	7.38	5.13	44.9

Parameter	Conditions		Typical values (T_A=25℃)				Maximum value (1) (T_A=105℃)	
			V_{DD}=2.4 V		V_{DD}= 3.3V		V_{DD}=3.6 V	
			I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)
Standby mode		Low-speed internal RC oscillator and independent watchdog ON	1.45	2.36	1.80	3.7	4.98	22.2
		Low-speed internal RC oscillator and independent watchdog OFF	1.10	1.93	1.31	3.05	4.44	21.5

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 32 VBAT Power Consumption

Symbol	Conditions	Typical value (1), T_A=25℃				Maximum value (1), V_{BAT}=3.6V		Unit
		V_{BAT}=2.0V	V_{BAT}=2.4V	V_{BAT}=3.3 V	V_{BAT}=3.6 V	T_A=25℃	T_A=105℃	
I_{DD_VBAT}	LSECLK and RTC ON, LSECLK oscillator drive capability configuration LSECLKDRV[1:0]=11	1.4	1.6	2.2	2.4	5.56	7.65	μA

Note:
(1) The data are obtained from a comprehensive evaluation and is not tested in production.

Peripheral power consumption

The HSECLK Bypass 1M is adopted as clock source, f_{PCLK}=f_{HCLK}=1M.

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table 33 Peripheral Power Consumption

Parameter	Peripheral	Typical value (1) T_A=25℃, V_{DD}=3.3V	Unit
Peripheral power consumption	CRC	0.86	μA/MHz
	DMA	3.88	
	GPIOA	3.45	
	GPIOB	3.83	
	GPIOC	0.875	
	GPIOD	0.5	
	GPIOF	0.41	
	SRAM	0.29	
	TSC	2.11	
	ALL_AHB	17.0	
	ADC	3.25	
	DAC	1.96	
	I2C1	8.25	
	I2C2	8.20	
	SPI1	8.08	
	SPI2	3.87	
	SYSCFG	2	
	TMR1	8	
	TMR3	6.16	
	TMR6	2.42	
	TMR14	3.62	
	TMR15	5.17	
	TMR16	4.08	
	TMR17	4.20	
	USART1	9.92	
	USART2	3.79	
	WWDG	1.79	
	ALL_APB	58.3	

5.3.5 Characteristics of external clock source

High-speed external clock generated by crystal resonator (HSECLK osc)

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 34 HSECLK4~32MHz Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistance	-	-	200	-	kΩ
I_{DD}	HSECLK current consumption	V_{DD} = 3.3 V, R_m = 45 Ω, C_L = 10 pF@8 MHz	-	660	-	μA
$t_{SU(HSECLK)}$	Startup time	V_{DD} is stable		1.7		ms

Note: Guaranteed by design and not tested in production.

Low-speed external clock generated by crystal resonator (LSECLK osc)

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 35 LSECLK Oscillator Characteristics (f_{LSECLK}=32.768KHz)

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
I_{DD}	LSECLK current consumption	High driving ability		1.5		μA
$t_{SU(LSECLK)}$(2)	Startup time	V_{DDIOx} is stable	-	2	-	s

Note:

(1) Guaranteed by design and not tested in production.

(2) $t_{SU(HSECLK)}$ is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

5.3.6 Characteristics of internal clock source

Test of high speed internal (HSICLK) RC oscillator

Table 36 HSICLK Oscillator Characteristics

Symbol	Parameter	Conditions		Minimum value	Typical values	Maximum value	Unit
f_{HSICLK}	Frequency	-		-	8	-	MHz
$A_{CC(HSICLK)}$	Accuracy of HSICLK oscillator	Factory calibration	V_{DD}=3.3V T_A=25℃	-1	-	1	%
			V_{DD}=2-3.6V T_A=-40~105℃	-5	-	5	%
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD}=3.3V T_A=-40~105℃		-	-	2	μs
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	-		-	60	-	μA

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 37 HSICLK14 Oscillator Characteristics

Symbol	Parameter	Conditions		Minimum value	Typical values	Maximum value	Unit
$f_{HSICLK14}$	Frequency	-		-	14	-	MHz
$A_{CCHSICLK14}$	Accuracy of HSICLK14 oscillator	Factory calibration	V_{DD}=3.3V T_A=25℃	-1	-	1	%
			V_{DD}=2-3.6V T_A=-40~105℃	-5	-	5	%
$t_{SU(HSICLK14)}$	Startup time of HSICLK14 oscillator	V_{DD}=3.3V T_A=-40~105℃		-	-	2	μs

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
$I_{DDA(HSICLK14)}$	Power consumption of HSICLK14 oscillator	-	-	72	-	μA

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Test of low speed internal (LSICLK) RC oscillator

Table 38 LSICLK Oscillator Characteristics

Symbol	Parameter	Minimum value	Typical values	Maximum value	Unit
f_{LSICLK}	Frequency (V_{DD}=2-3.6V, T_A=-40~105℃)	30	40	50	KHz
$t_{SU(LSICLK)}$	Startup time of LSICLK oscillator（V_{DD}=3.3V，T_A=-40~105℃）	-	30	-	μs
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator	-	0.5	-	μA

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.3.7 Wake-up time in low power mode

Table 39 Awakening Clock Source Parameters

Symbol	Parameter	Typical values	Unit
$t_{WUSLEEP}$	Wake-up from sleep mode	4 SYSCLK cycles	μs
t_{WUSTOP}	Wake up from stop mode	3.1	
$t_{WUSTDBY}$	Wake up from standby mode	40	

Note: The wake-up time is measured from the start of the wake-up event to the first instruction read by the user program.

5.3.8 PLL Characteristics

Table 40 PLL Characteristics

Symbol	Parameter	Numerical value (1)			Unit
		Minimum value	Typical values	Maximum value	
f_{PLL_IN}	PLL input clock	1	8	24	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL frequency doubling output clock (V_{DD}=3.3V，T_A=-40~105℃）	16	-	48	MHz
t_{LOCK}	PLL phase locking time	-	-	90	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.3.9 Memory characteristics

FLASH memory

Table 41 FLASH Memory Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
t_{prog}	16-bit programming time	T_A =-40~105℃ V_{DD}=2.0~3.6V	-	17.9	-	μs
t_{ERASE}	Page (1KB) erase time	T_A=-40~105℃ V_{DD}=2.0~3.6V	-	1.56	-	ms
t_{ME}	Whole erase time	T_A=25℃ V_{DD}=3.3V	-	6.4	-	ms
V_{prog}	Programming voltage	T_A=-40~105℃	2.0	3.3	3.6	V
t_{RET}	Data saving time	T_A=125℃	18	-	-	years
N_{RW}	Erase cycle	T_A=25℃	100K	-	-	cycles

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.3.10 I/O port characteristics

Table 42 DC Characteristics (TA=-40℃-105℃,VDD=2~3.6V)

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{IL}		TC and TTa I/O	-	-	$0.3V_{DD}$+0.1	V
		FT and FTf I/O	-	-	$0.476V_{DD}$-0.4	

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
	Low level input voltage	I/O pins except BOOT0 pin	-	-	$0.3V_{DD}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.447V_{DD}+0.402$	-	-	V
		FT and FTf I/O	$0.5V_{DD}+0.2$	-	-	
		I/O pins except BOOT0 pin	$0.7V_{DD}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O		200		mV
		FT and FTf I/O		300		
I_{lkg}	Input leakage current	TC, FT and FTf I/O TTa in digital mode $V_{SS}\leq V_{IN}\leq V_{DDIOx}$	-	-	±0.1	μA
		TTa in digital mode $V_{DDIOx}\leq V_{IN}\leq V_{DDA}$	-	-	1	
		TTa in analog mode $V_{DDIOx}\leq V_{IN}\leq V_{DDA}$	-	-	±0.1	
		FT and FTf I/O (1) $V_{DDIOx}\leq V_{IN}\leq 5V$	-	-	10	
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistance	$V_{IN}=V_{DDIOx}$	30	40	50	kΩ

Table 43 AC Characteristics (TA =25℃)

MODEx[1:0] Configuration	Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
10 (2MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50 pF, V_{DD}=2.4~3.6V	-	2	MHz
	$t_{f(IO)out}$	Output fall time from high to low level	C_L=50 pF, V_{DD}=2.4~3.6V	-	125	ns
	$t_{r(IO)out}$	Output rise time from low to high level		-	125	
01 (10MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50 pF, V_{DD}=2.4~3.6V	-	10	MHz
	$t_{f(IO)out}$	Output fall time from high to low level	C_L=50 pF, V_{DD}=2.4~3.6V	-	25	ns
	$t_{r(IO)out}$	Output rise time from low to high level		-	25	
11 (50MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=30 pF, V_{DD}=2.7~3.6V	-	50	MHz
	$t_{f(IO)out}$	Output fall time from high to low level	C_L=30 pF, V_{DD}=2.7~3.6V	-	5	ns
	$t_{r(IO)out}$	Output rise time from low to high level		-	5	
FM+ configuration	$f_{max(IO)out}$	Maximum frequency (3)	C_L=50pF, V_{DDIOx} =2.4~3.6V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	34	ns
	$t_{r(IO)out}$	Output rise time		-	34	

Figure 12 I/O AC Characteristics Definition

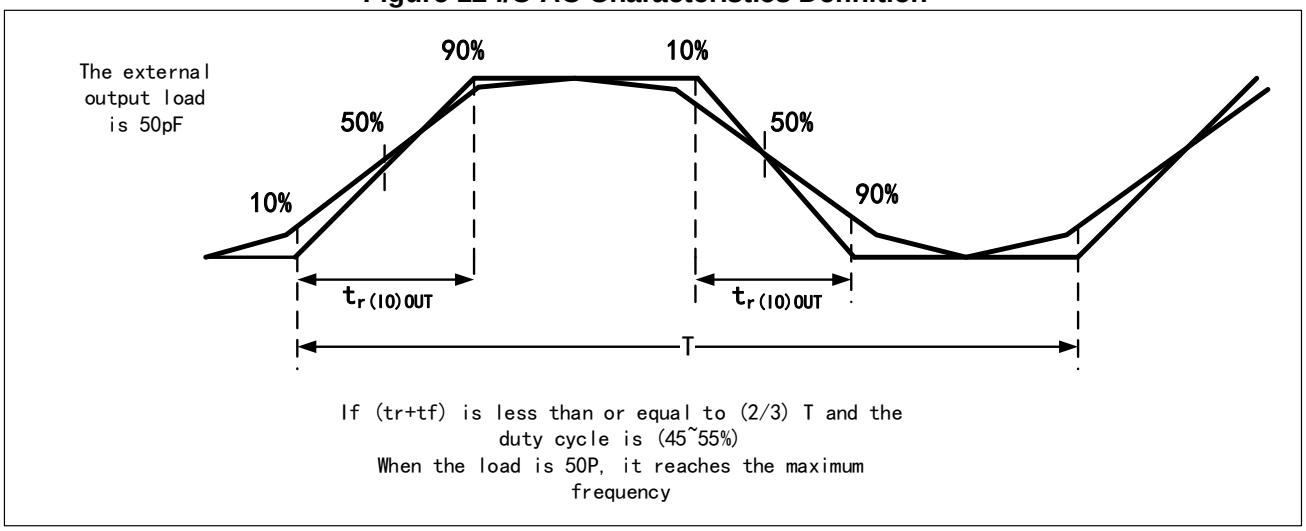


Table 44 Output Drive Current Characteristics (TA =25℃)

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=8 mA	-	0.4	V
V_{OH}	I/O pin outputs high voltage	V_{DDIOx}≥2.7V	V_{DDIOx}-0.4	-	
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=20 mA	-	1.3	V
V_{OH}	I/O pin outputs high voltage	V_{DDIOx}≥2.7V	V_{DDIOx}-1.3	-	

5.3.11 NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}.

Table 45 NRST Pin Characteristics (TA=-40℃-105℃,VDD=2~3.6V)

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
$V_{IL(NRST)}$	NRST low level input voltage	-	-	-	$0.31V_{DD}$+0.065	V
$V_{IH(NRST)}$	NRST high level input voltage	-	$0.446V_{DD}$+0.405			
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	300	-	mV
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ

5.3.12 Communication interface

I2C interface characteristics

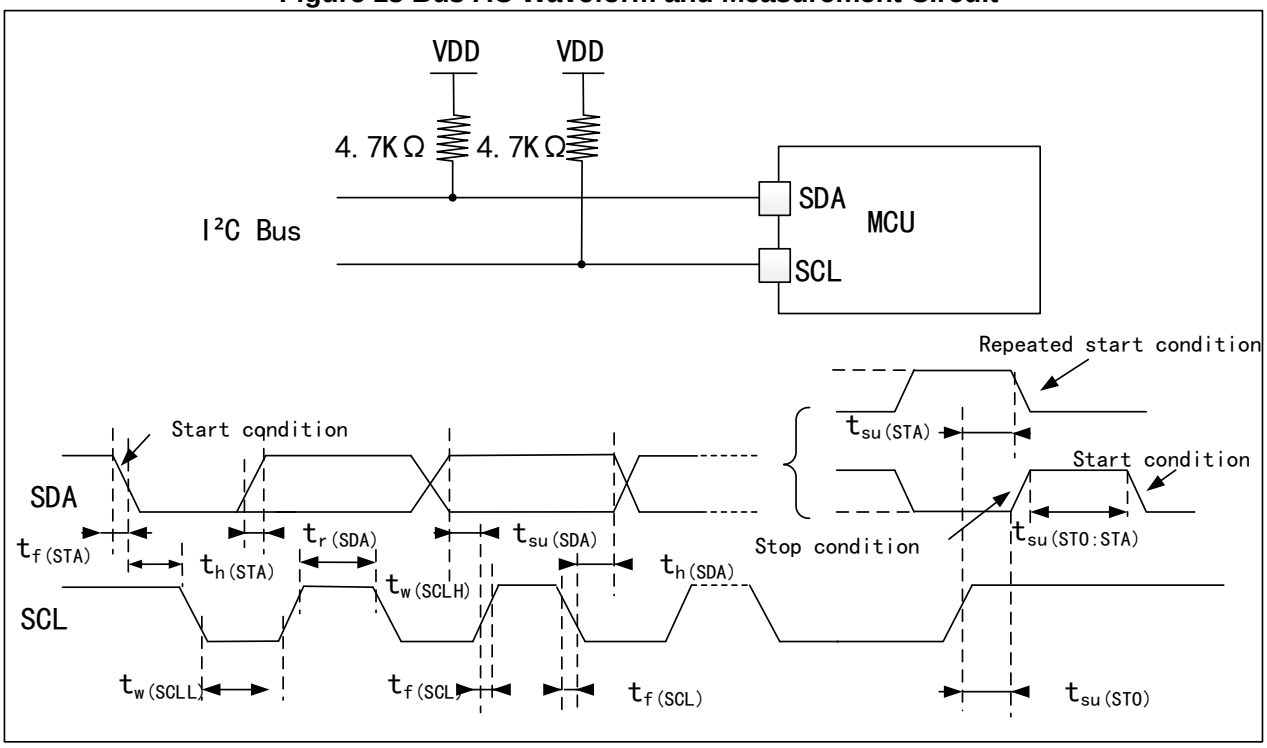
- Standard mode (Sm): Up to 100kbit/s
- Fast mode (Fm): Up to 400 kbit/s
- Ultra fast mode (Fm+): Up to 1 Mbit/s

Table 46 I2C Interface Characteristics (TA=25℃, VDD=3.3V)

Symbol	Parameter	Standard I2C		Fast I2C		Ultra fast I2C		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	Minimum value	Maximum value	
$t_{w(SCLL)}$	SCL clock low time	4.84	-	1.21	-	0.52	-	μs
$t_{w(SCLH)}$	SCL clock high time	5.09	-	1.14	-	0.46	-	
$t_{su(SDA)}$	SDA setup time	4460	-	860	-	321	-	ns

Symbol	Parameter	Standard I2C		Fast I2C		Ultra fast I2C		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	Minimum value	Maximum value	
$t_{h(SDA)}$	SDA data hold time	-	3450	0	252	0	145	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	500	-	300	-	120	
$t_{f(SDA)}$ /$t_{f(SCL)}$	SDA and SCL fall time	-	9.86	-	8.12	-	4	
$t_{h(STA)}$	Start condition hold time	4.96	-	1		0.33	-	μs
$t_{su(STA)}$	Repeated start condition setup time	5.16	-	1.21	-	0.64	-	
$t_{su(STO)}$	Setup time of stop condition	4.50	-	1.21	-	0.54	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.67	-	1.37	-	0.77	-	μs

Figure 13 Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

SPI interface characteristics

Table 47 SPI Characteristics (T_A =25℃,V_{DD}=3.3V)

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SI clock rise and fall time	Load capacitance: C = 15pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	223		ns
$t_{h(NSS)}$	NSS hold time	Slave mode	65		ns
$t_{w(SCKH)}$	SCK high and low time	Main mode, f_{PCLK} = 36MHz,	54	57	ns

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
$t_{w(SCKL)}$		Prescaler factor=4			
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	12		ns
		Slave mode	20		
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	34		ns
		Slave mode	22		
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20MHz		17	ns
$t_{dis(SO)}$	Data output prohibition time	Slave mode		18	ns
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)		16	ns
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)		6	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	11.5		ns
$t_{h(MO)}$		Master mode (after enable edge)	2		

Figure 14 SPI Timing Diagram - Slave Mode and CPHA=0

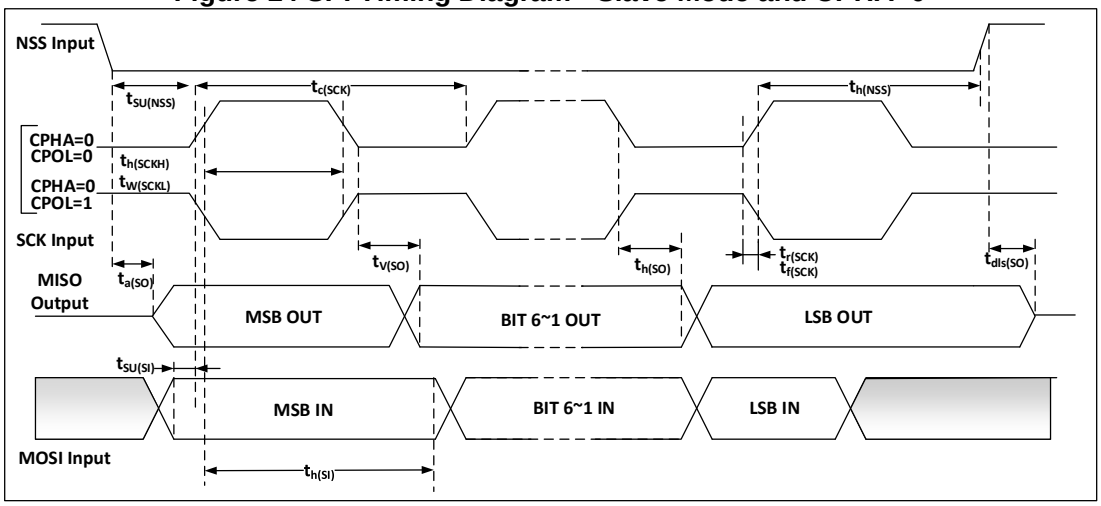
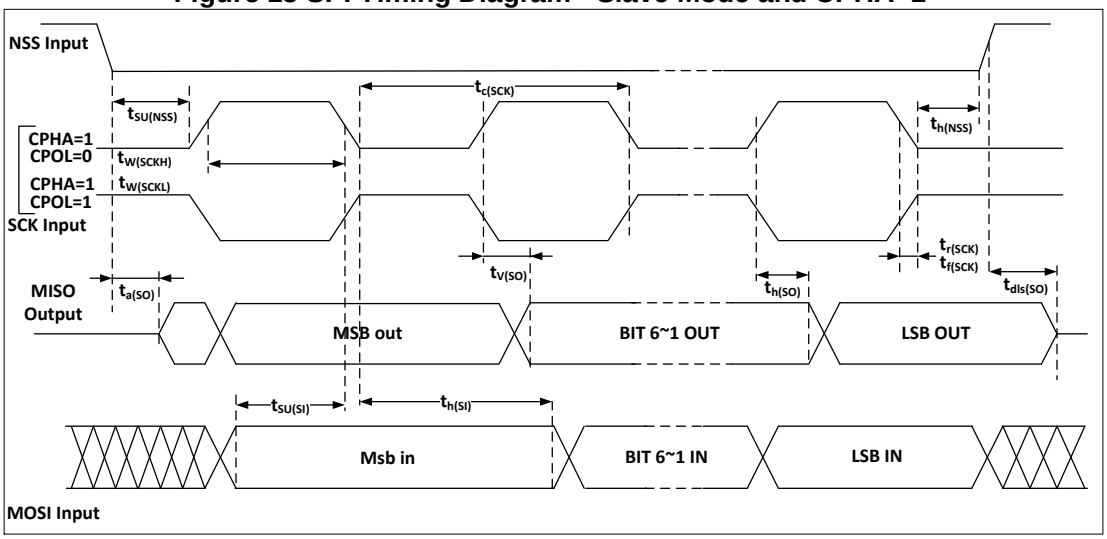
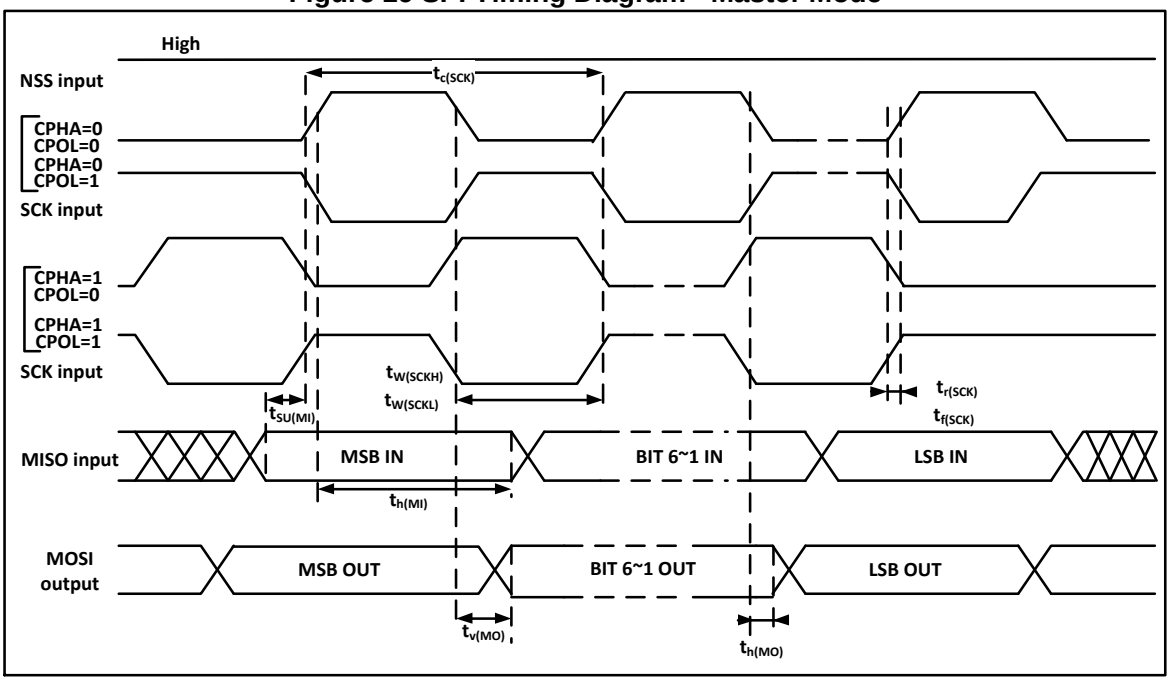


Figure 15 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 16 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.13 12-bit ADC characteristics

Table 48 12-bit ADC Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{DDA}	Power supply voltage	-	2.4	-	3.6	V
f_{ADC}	ADC frequency	-	0.6	-	14	MHz
C_{ADC}	Internal sampling and holding capacitance	-	-	8	-	pF
R_{ADC}	Sampling resistor	-	-	-	1000	Ω
t_S	Sampline Time	f_{ADC} = 14 MHz	0.107	-	17.1	μs
T_{CONV}	Sampling and conversion Time	f_{ADC} = 14 MHz, 12-bit conversion	1	-	18	μs

Table 49 12-bit ADC Accuracy

Symbol	Parameter	Conditions	Typical values	Maximum value	Unit
$\|E_T\|$	Composite error	f_{PCLK}=48MHz, f_{ADC}=14MHz, V_{DDA}=2.4V-3.6V T_A=-40℃~105℃	3.4	4.0	LSB
$\|E_O\|$	Offset error		2.1	3	
$\|E_G\|$	Gain error		0.6	1.3	
$\|E_D\|$	Differential linear error		0.65	1.3	
$\|E_L\|$	Integral linear error		1.32	1.65	

5.3.14 DAC Characteristics

Test parameter description:

- DNL differential non-linear error: the deviation between two consecutive codes is—— 1 LSB
- INL integral non-linear error: the difference between the measured value at code i and the value at code i on the connection between code 0 and the last code 4095

Table 50 DAC Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit

V_{DDA}	Analog power supply voltage	-	2.4	-	3.6	V
R_{LOAD}	Resistive load	Load is connected to V_{SSA} with buffer on	5	-	-	kΩ
		Load is connected to V_{DDA} with buffer on	-	-	-	
RO	Output impedance	The resistive load between DAC_OUT and VSS is 1.5MΩ with buffer off	-	-	15	kΩ
C_{LOAD}	Capacitive load	Maximum capacitive load at DAC_OUT pin with buffer on	-	-	50	pF
DAC_OUT	The voltage of DAC_OUT output	The buffer is on, corresponding to the 12-bit input codes (0x0E0) to (0xF1C) when V_{DDA}=3.6V and (0x155) and (0xEAB) when V_{DDA}=2.4V	0.2	-	$V_{DDA-0.2}$	V
		The buffer is off, corresponding to the 12-bit input codes (0x0E0) to (0xF1C) when VDDA=3.6V and (0x155) and (0xEAB) when VDDA=2.4V	-	0.5	$V_{DDA-1LSB}$	mV
I_{DDA}	Power consumption of DAC in quiescent mode	Non-load, the input terminal adopts intermediate code (0x800)	-	-	295	uA
		Non-load, the input terminal adopts difference code (0xF1C)			340	
DNL	Differential non-linear error	Configured with 12-bit DAC	-	-	±2	LSB
INL	Integral non-linear error	Configured with 12-bit DAC	-	-	±4	LSB
Offset	Offset error	V_{DDA}=3.6 is configured with12-bit DAC	-	-	±10	LSB
Gain error	Gain error	Configured with 12-bit DAC	-	-	±0.4	%

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.3.15 Comparator (COMP)

Table 51 Comparator Characteristics

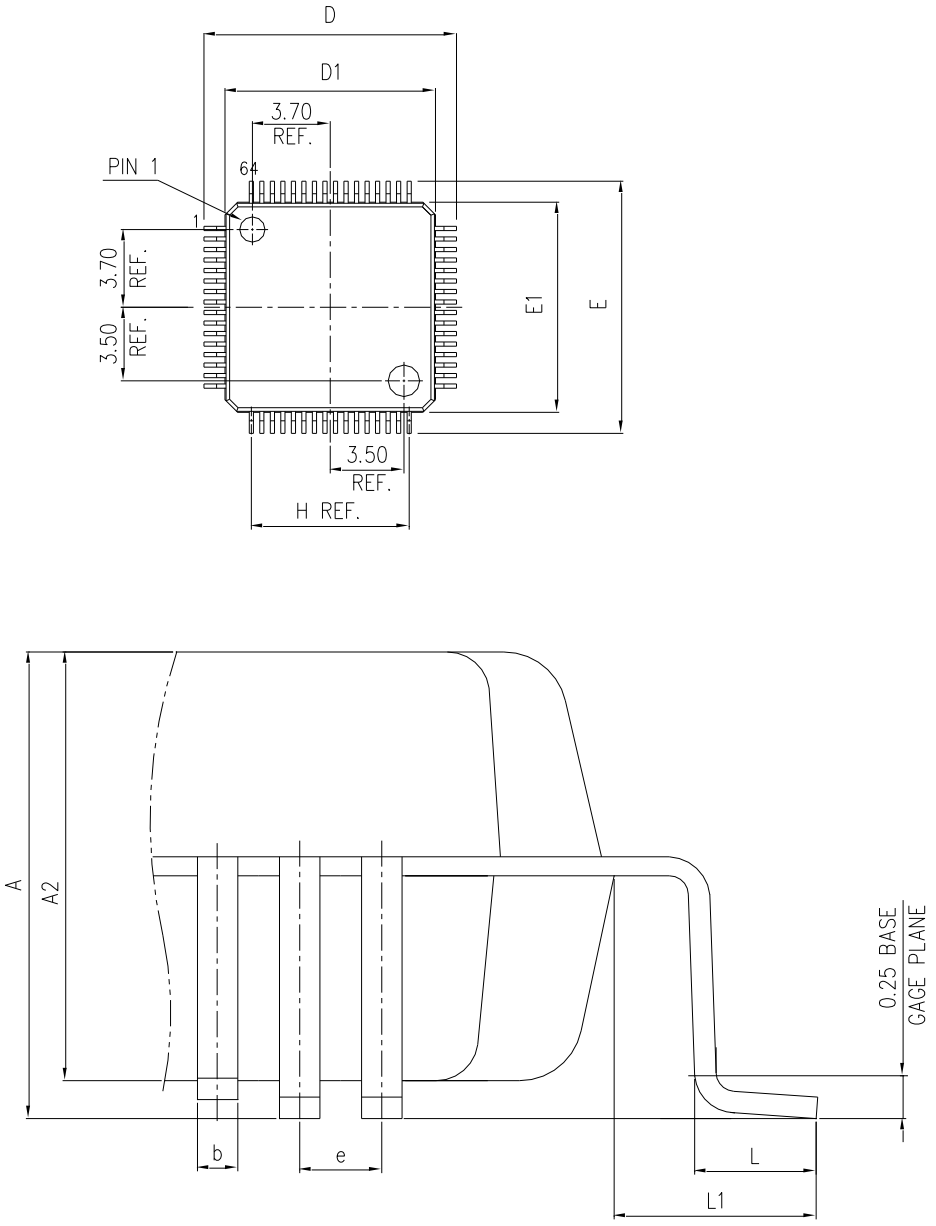
Symbol	Parameter	Conditions		Minimum value	Typical values	Maximum value	Unit
V_{DDA}	Analog power supply voltage	-		VDD	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	VDDA	-
t_D	Full range step, overload propagation delay of 100mV	Very low power mode		-	2	7	μs
		Low-power mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		Full speed mode	VDDA≥2.7V	-	90	180	ns
			VDDA＜2.7V	-	110	300	
V_{OFFSET}	Offset error	-		-	+4	±10	mv

Note: It is obtained from a comprehensive evaluation and is not tested in production.

6 Package information

6.1 LQFP64 package information

Figure 17 LQFP64 Package Diagram



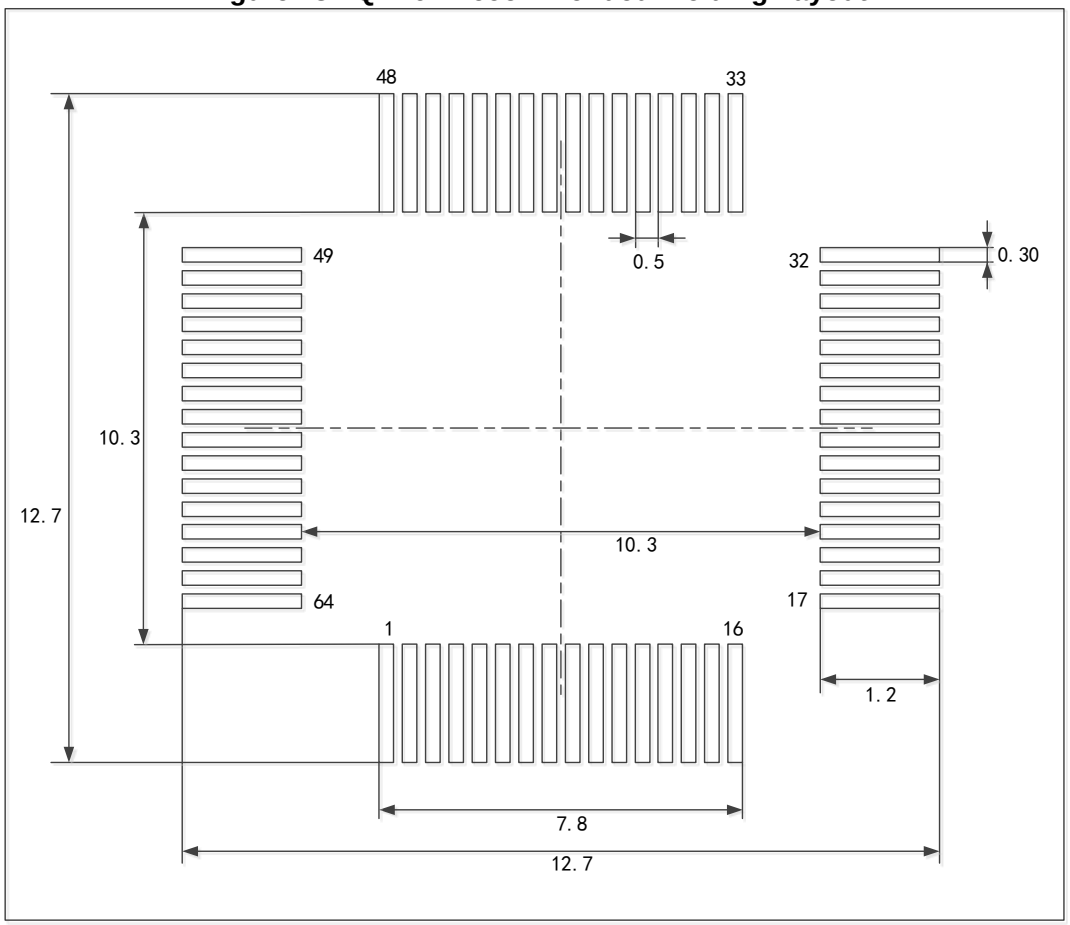
Note: The figure is not drawn to scale.

Table 52 LQFP64 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	12.000±0.200	LEAD TIP TO TIP
4	D1	10.000±0.100	PKG LENGTH
5	E	12.000±0.200	LEAD TIP TO TIP
6	E1	10.000±0.100	PKG WIDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF.	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H(REF.)	(7.500)	GUM.LEAD PITCH
11	b	0.220±0.050	LEAD WIDTH

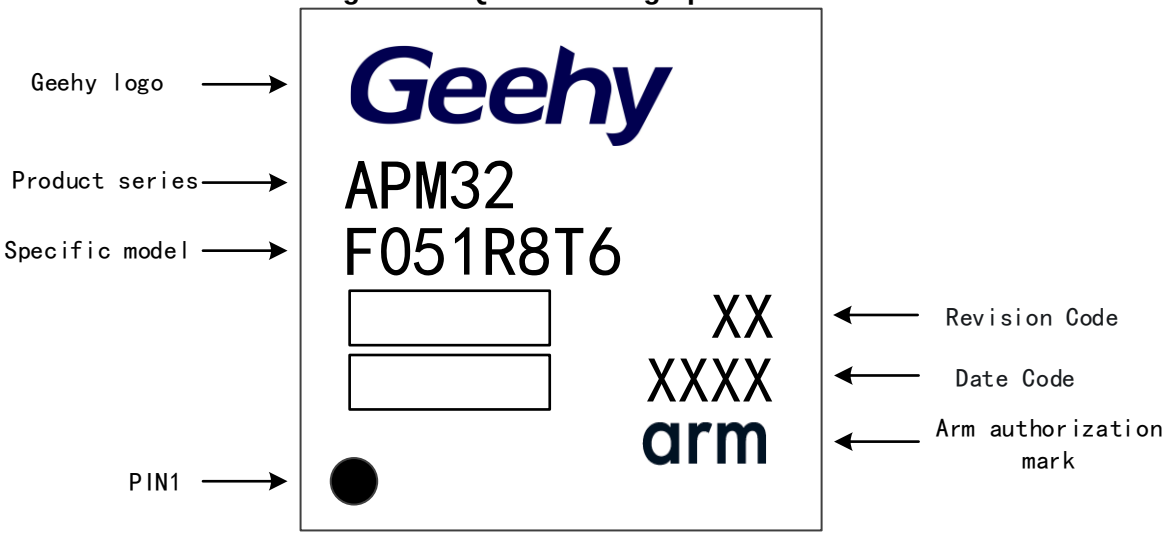
Note: The value in inches is converted from mm to 4 decimal places.

Figure 18 LQFP64 Recommended Welding Layout



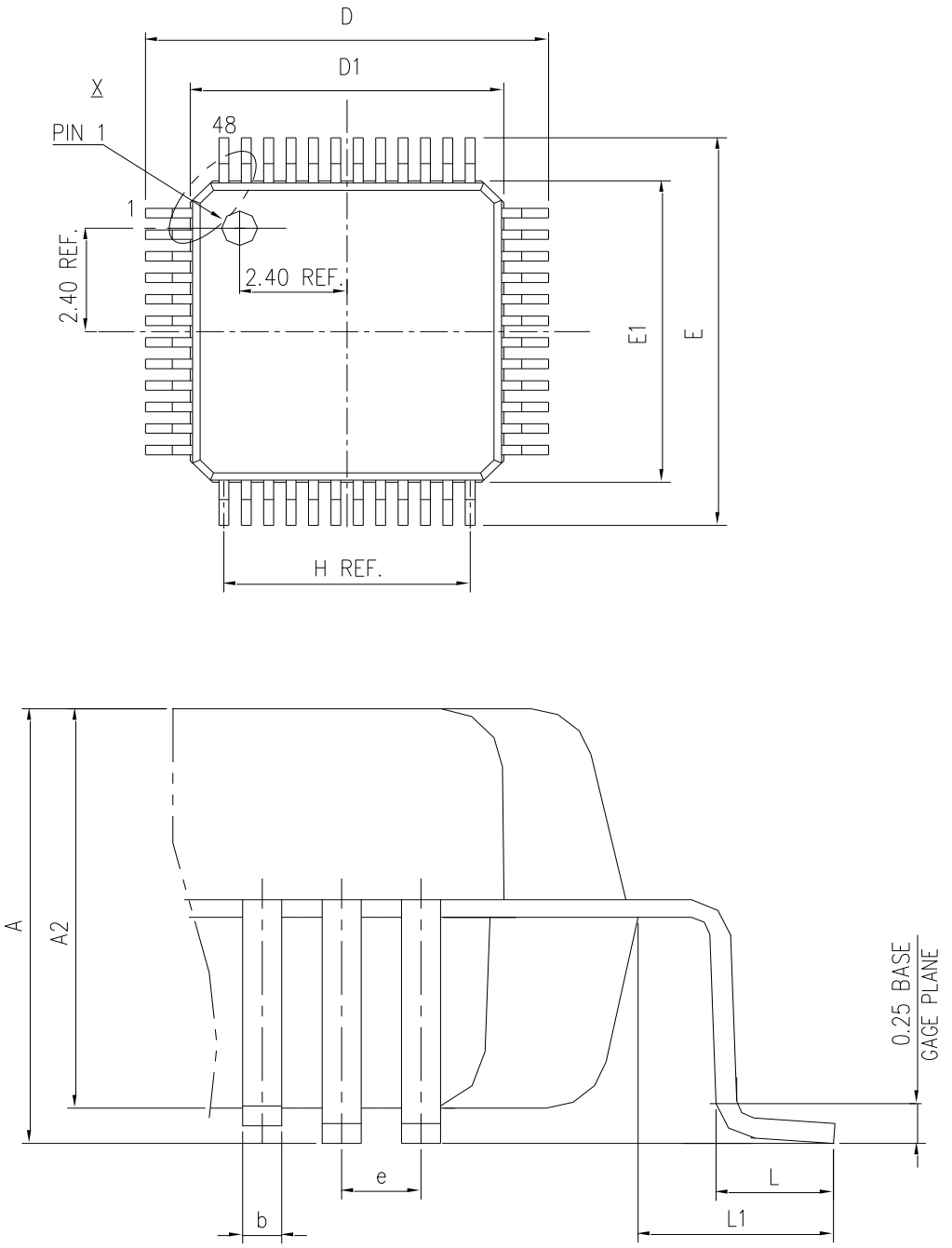
Note: Dimensions are marked in millimeters.

Figure 19 LQFP64 Coding Specification



6.2 LQFP48 package information

Figure 20 LQFP48 Package Diagram



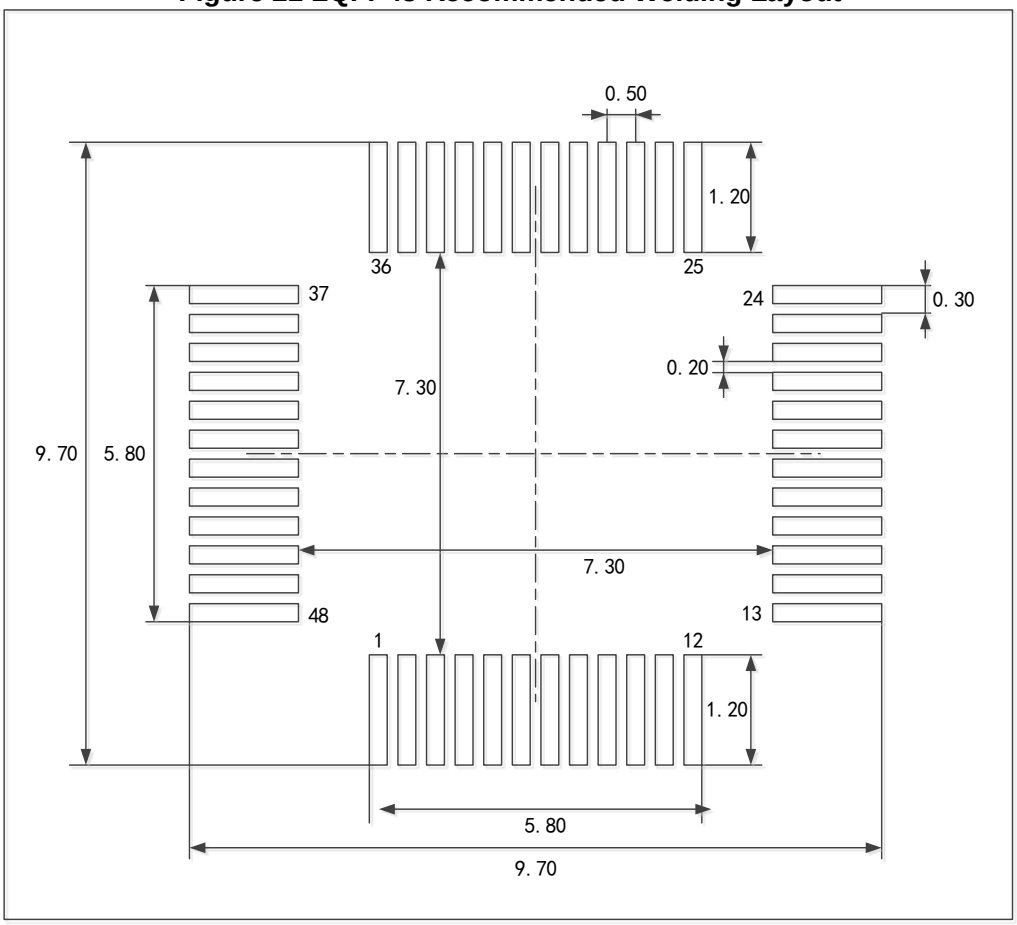
Note: The figure is not drawn to scale.

Table 53 LQFP48 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.60	OVERALL HEIGHT
2	A2	1.40±0.05	PKG THICKNESS
3	D	9.00±0.20	LEAD TIP TO TIP
4	D1	7.00±0.10	PKG LENGTH
5	E	9.00±0.20	LEAD TIP TO TIP
6	E1	7.00±0.10	PKG WIDTH
7	L	0.60±0.15	FOOT LENGTH
8	L1	1.00 REF.	LEAD LENGTH
9	e	0.50 BASE	LEAD PITCH
10	H(REF.)	（ 5.50 ）	GUM.LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

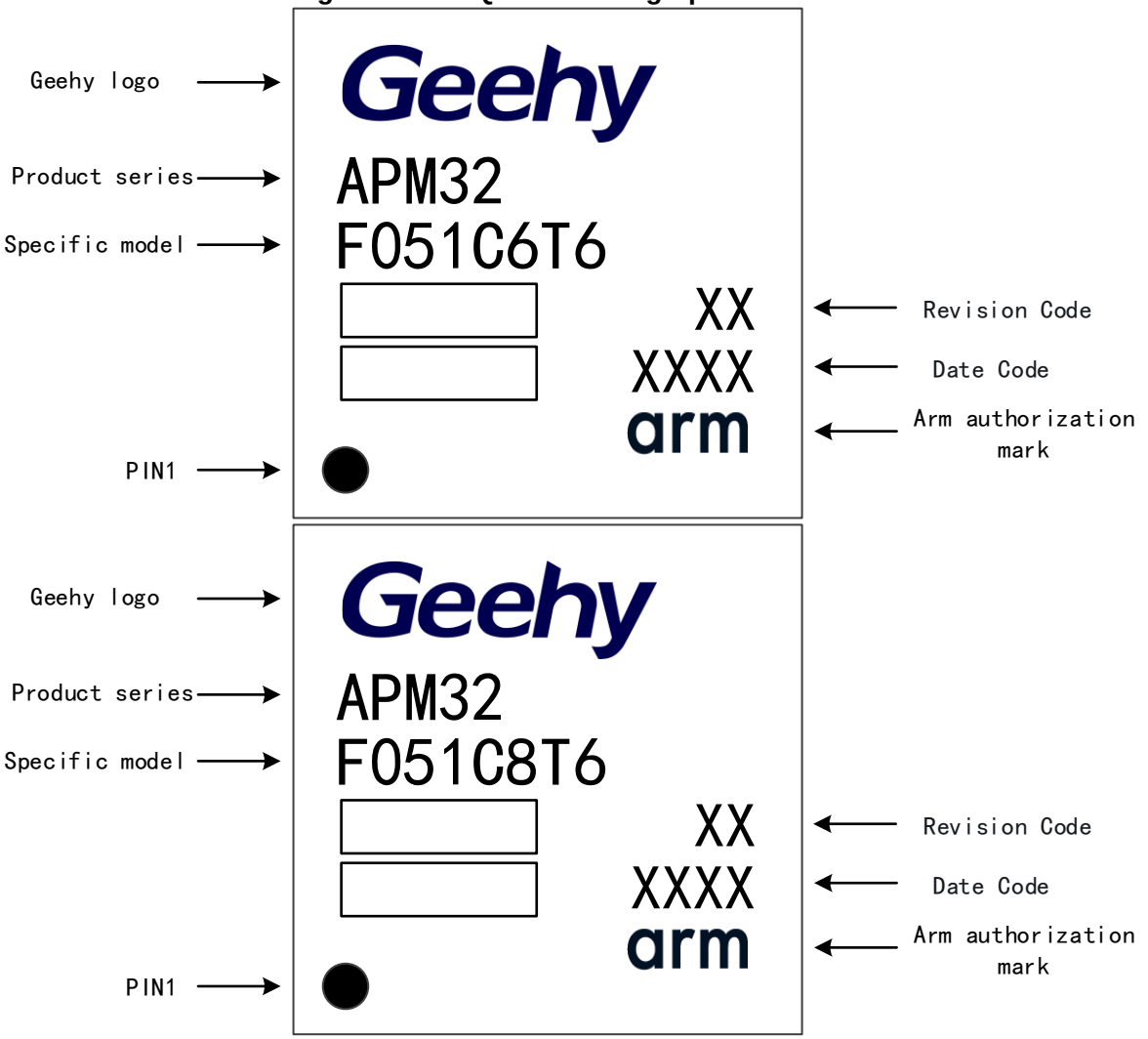
Note: The value in inches is converted from mm to 4 decimal places.

Figure 21 LQFP48 Recommended Welding Layout



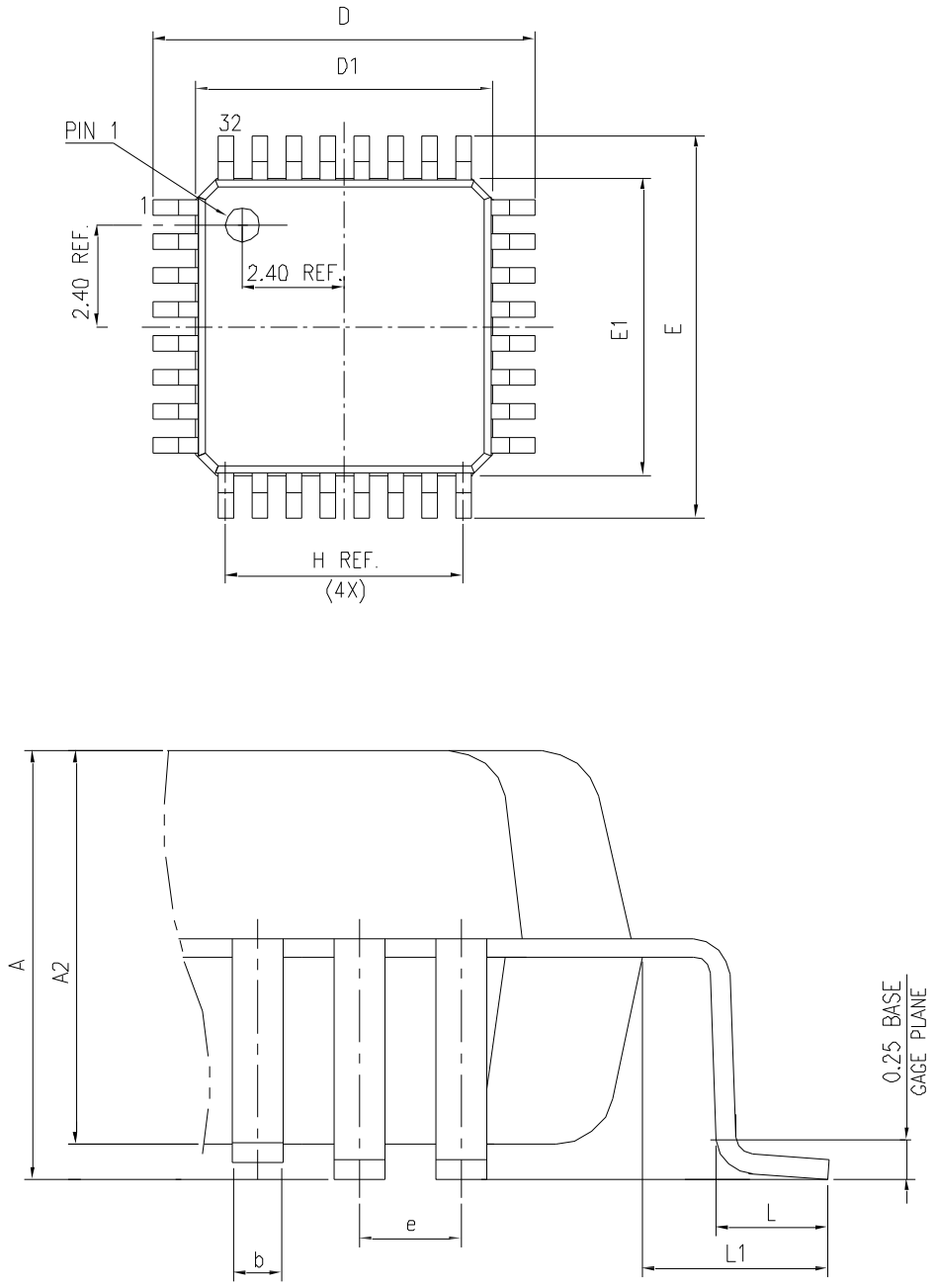
Note: Dimensions are marked in millimeters.

Figure 1 LQFP48 Coding Specification



6.3 LQFP32 package information

Figure 22 LQFP32 Package Diagram



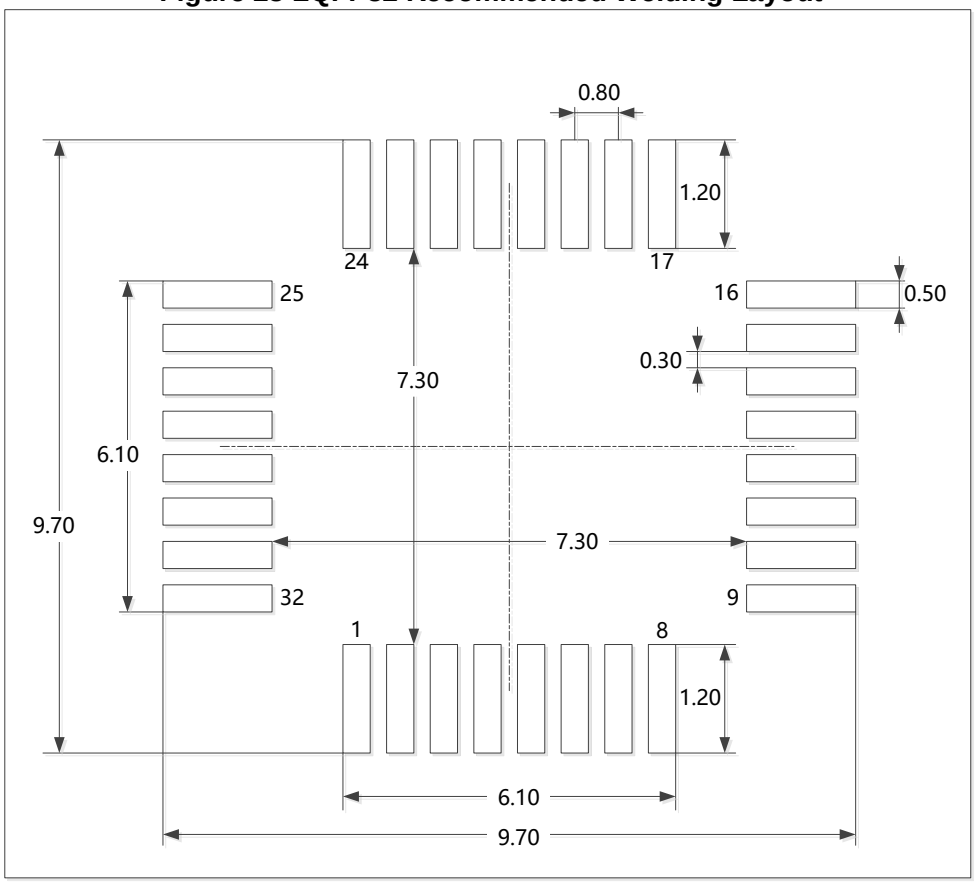
Note: The figure is not drawn to scale.

Table 54 LQFP32 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.6	OVERALL HEIGHT
2	A2	1.40±0.05	PKG THICKNESS
3	D	9.00±0.20	LEAD TIP TO TIP
4	D1	7.00±0.10	PKG LENGTH
5	E	9.00±0.20	LEAD TIP TO TIP
6	E1	7.00±0.10	PKG WIDTH
7	L	0.60±0.15	FOOT LENGTH
8	L1	1.00 REF.	LEAD LENGTH
9	e	0.80 BASE	LEAD PITCH
10	H(REF.)	（ 5.60 ）	GUM.LEAD PITCH
11	b	0.370±0.080/0.070	LEAD WIDTH

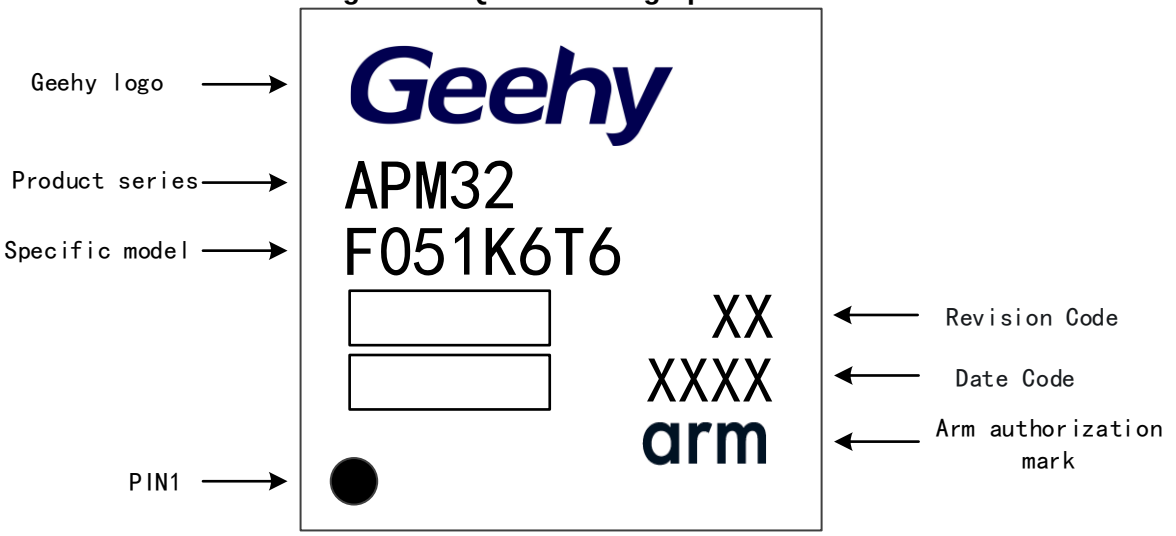
Note: The value in inches is converted from mm to 4 decimal places.

Figure 23 LQFP32 Recommended Welding Layout



Note: Dimensions are marked in millimeters.

Figure 24 LQFP32 Coding Specification



6.4 QFN48 package information

Figure 25 QFN48 Package Diagram

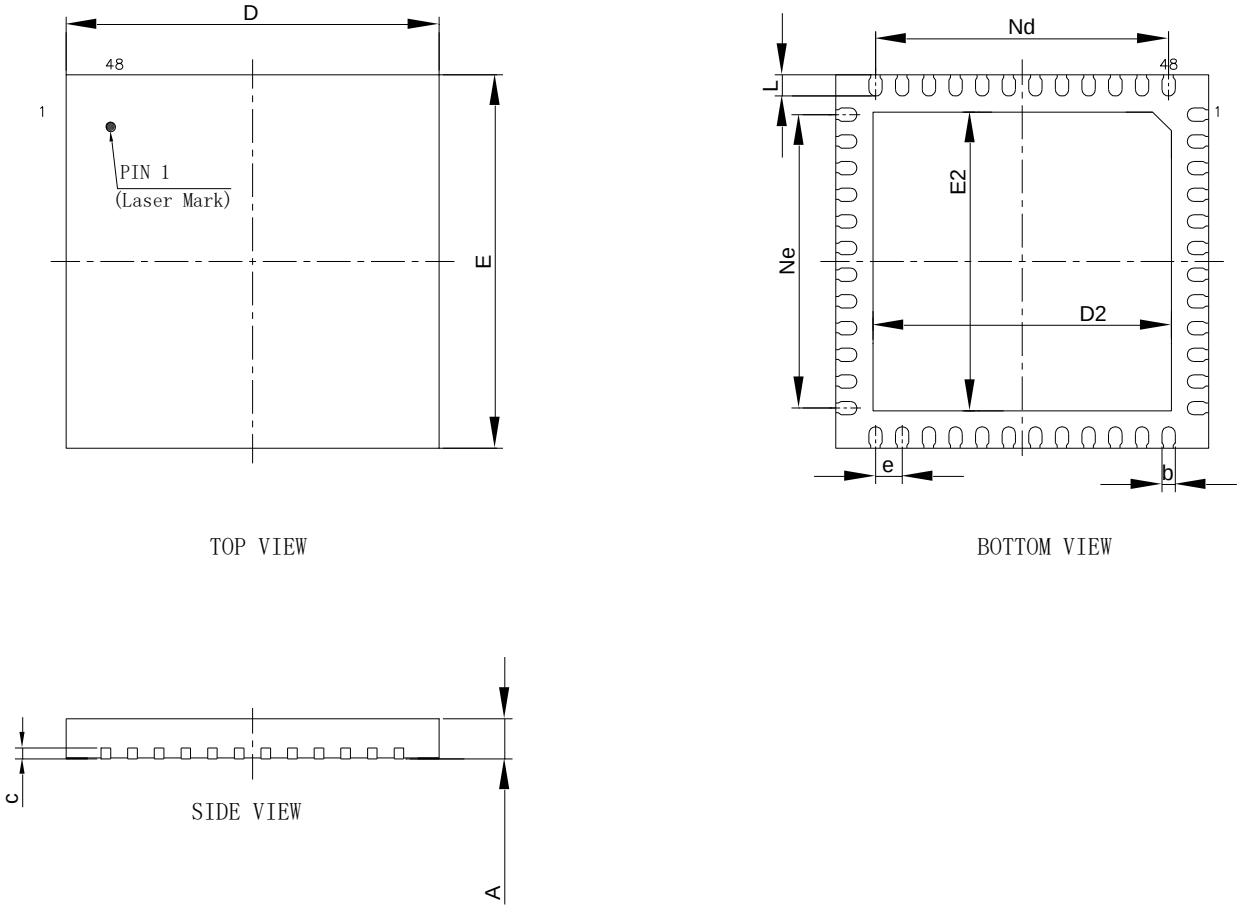


Table 55 QFN48 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.203REF		
e	0.50BSC		
Ne	5.50BSC		
Nd	5.50BSC		
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
L	0.35	0.40	0.45

Note: Dimensions are marked in millimeters.

Figure 26 QFN48 recommended welding layout

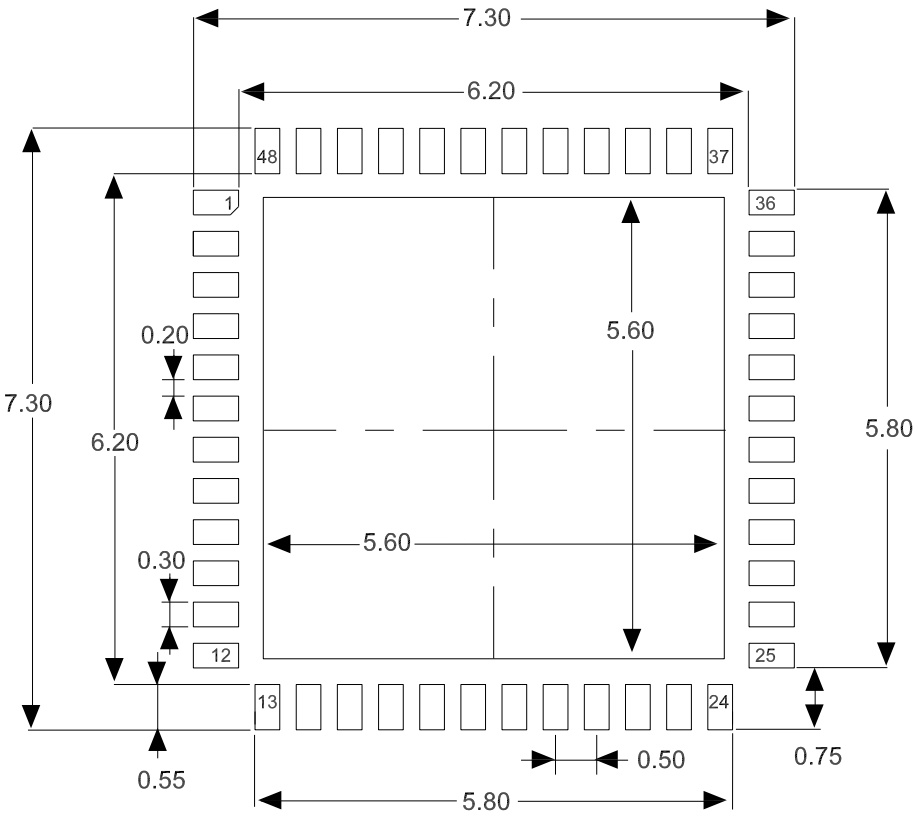
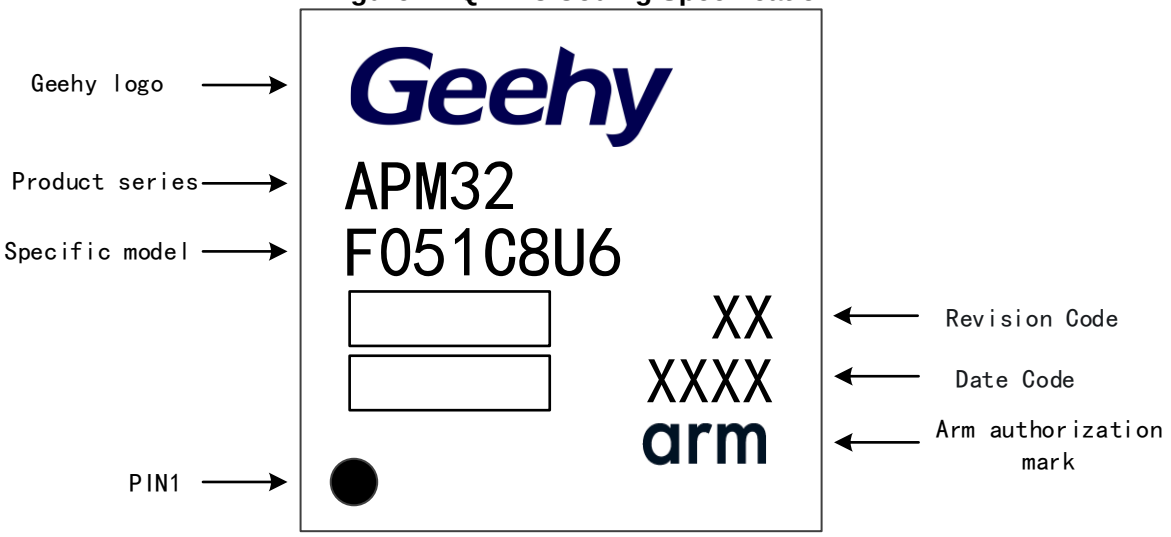


Figure 27 QFN48 Coding Specification



6.5 QFN32 package information

Figure 28 QFN32 Package Diagram

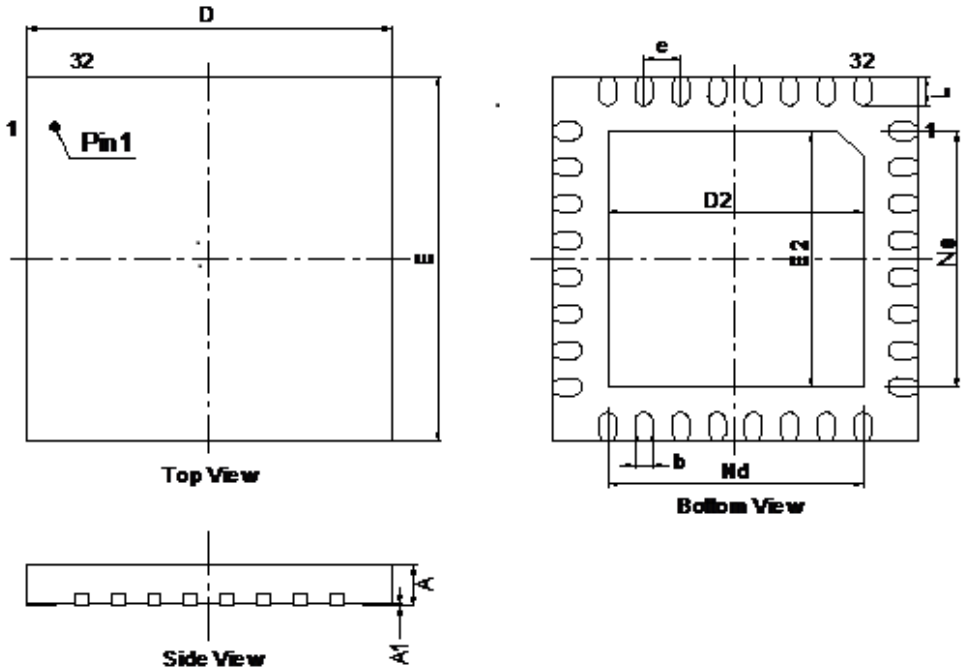


Table 56 QFN32 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.5	0.55	0.6
A1	0	0.02	0.05
b	0.19	0.24	0.29
D	4.9	5	5.1
D2	3.4	3.5	3.6
e	0.50BSC		
Nd	3.50BSC		
E	4.9	5	5.1
E2	3.4	3.5	3.6
Ne	3.50BSC		
L	0.35	0.4	0.45

Figure 29 QFN32 Recommended Welding Layout

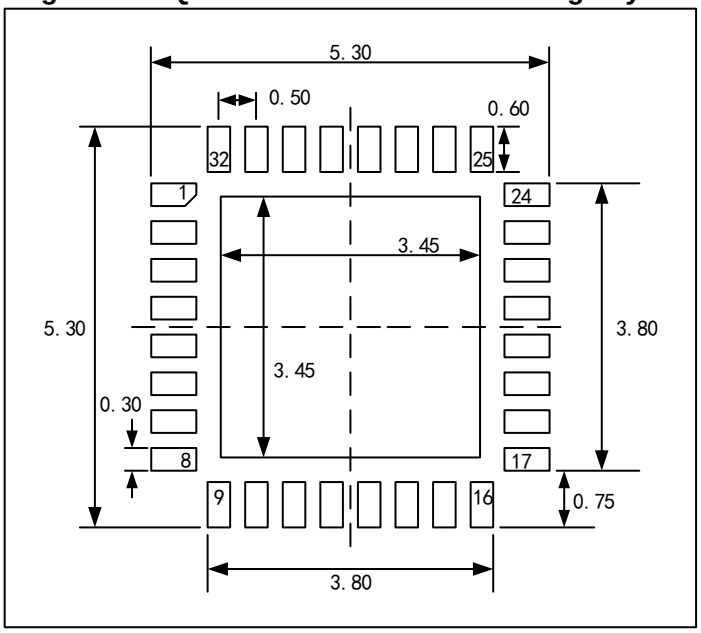
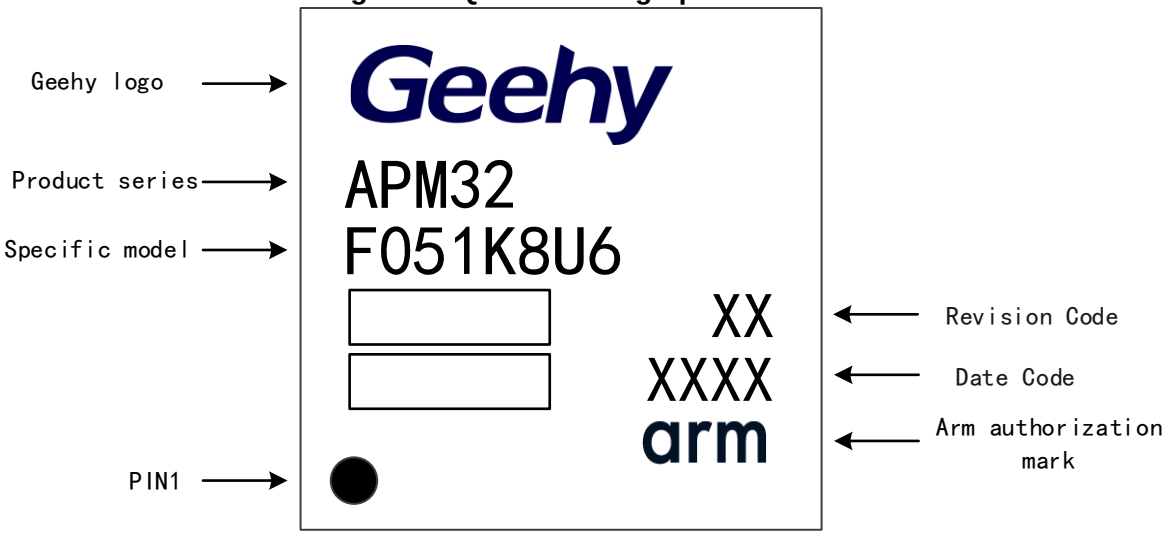


Figure 30 QFN32 Coding Specification



7 Ordering Information

Figure 31 Product Naming Rules

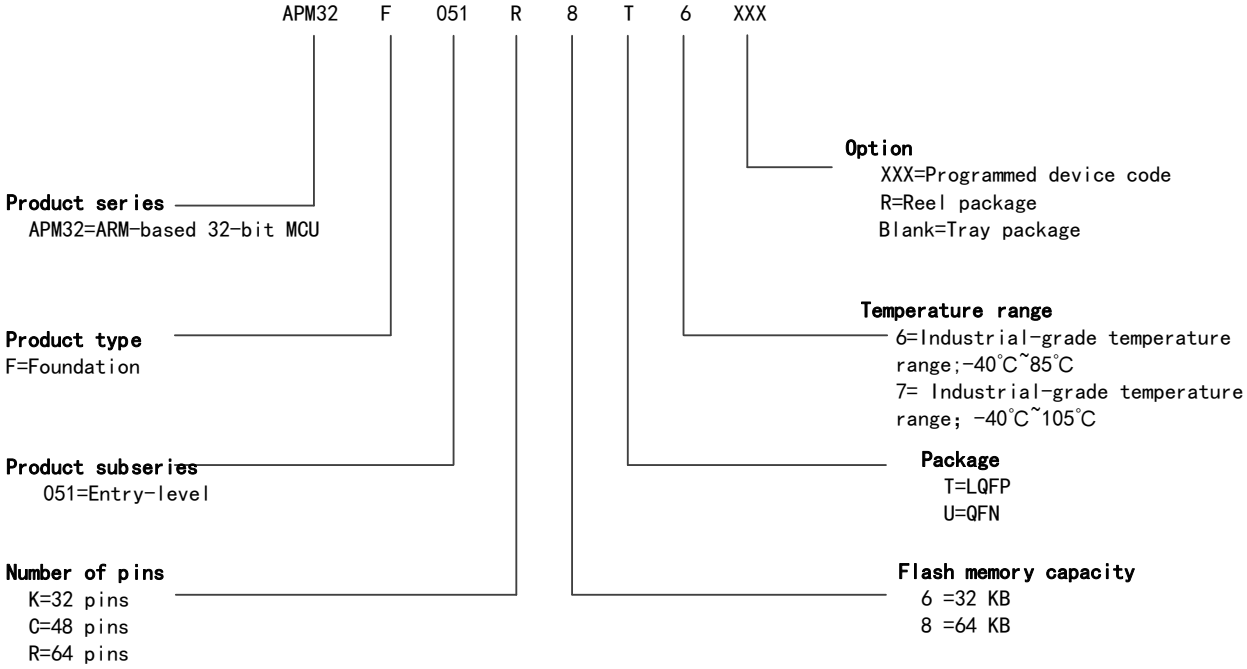


Table 57 Ordering Information Table

Order Code	FLASH(KB)	SRAM(KB)	Package	SPQ	Temperature Range
APM32F051K6U6-R	32	8	QFN32	5000	Industrial grade -40℃~85℃
APM32F051K6U6	32	8	QFN32	4900	Industrial grade -40℃~85℃
APM32F051K8U6-R	64	8	QFN32	5000	Industrial grade -40℃~85℃
APM32F051K8U6	64	8	QFN32	4900	Industrial grade -40℃~85℃
APM32F051C6U6-R	32	8	QFN48	2500	Industrial grade -40℃~85℃
APM32F051C6U6	32	8	QFN48	2600	Industrial grade -40℃~85℃
APM32F051C8U6-R	64	8	QFN48	2500	Industrial grade -40℃~85℃
APM32F051C8U6	64	8	QFN48	2600	Industrial grade -40℃~85℃
APM32F051K6T6-R	32	8	LQFP32	2000	Industrial grade -40℃~85℃
APM32F051K6T6	32	8	LQFP32	2500	Industrial grade -40℃~85℃
APM32F051K8T6-R	64	8	LQFP32	2000	Industrial grade -40℃~85℃
APM32F051K8T6	64	8	LQFP32	2500	Industrial grade -40℃~85℃
APM32F051C6T6-R	32	8	LQFP48	2000	Industrial grade -40℃~85℃
APM32F051C6T6	32	8	LQFP48	2500	Industrial grade -40℃~85℃
APM32F051C8T6-R	64	8	LQFP48	2000	Industrial grade -40℃~85℃
APM32F051C8T6	64	8	LQFP48	2500	Industrial grade -40℃~85℃
APM32F051R6T6-R	32	8	LQFP64	1000	Industrial grade -40℃~85℃
APM32F051R6T6	32	8	LQFP64	1600	Industrial grade -40℃~85℃

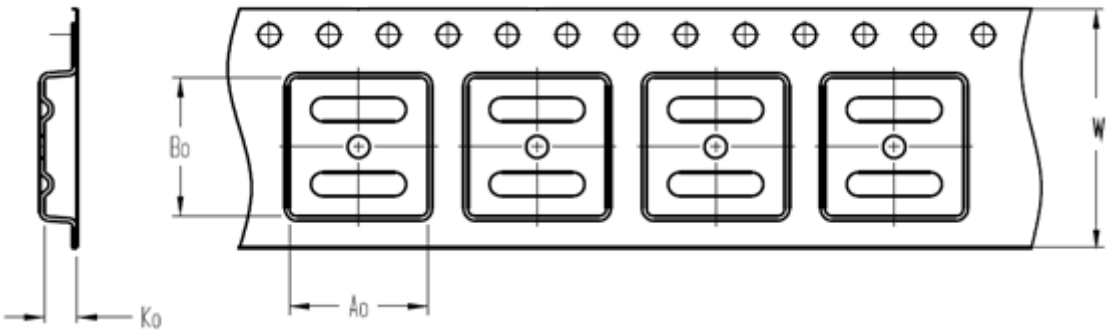
Order Code	FLASH(KB)	SRAM(KB)	Package	SPQ	Temperature Range
APM32F051R8T6-R	64	8	LQFP64	1000	Industrial grade -40℃~85℃
APM32F051R8T6	64	8	LQFP64	1600	Industrial grade -40℃~85℃
APM32F051K6U7-R	32	8	QFN32	5000	Industrial grade -40℃~105℃
APM32F051K6U7	32	8	QFN32	4900	Industrial grade -40℃~105℃
APM32F051K8U7-R	64	8	QFN32	5000	Industrial grade -40℃~105℃
APM32F051K8U7	64	8	QFN32	4900	Industrial grade -40℃~105℃
APM32F051C6U7-R	32	8	QFN48	2500	Industrial grade -40℃~105℃
APM32F051C6U7	32	8	QFN48	2600	Industrial grade -40℃~105℃
APM32F051C8U7-R	64	8	QFN48	2500	Industrial grade -40℃~105℃
APM32F051C8U7	64	8	QFN48	2600	Industrial grade -40℃~105℃
APM32F051K6T7-R	32	8	LQFP32	2000	Industrial grade -40℃~105℃
APM32F051K6T7	32	8	LQFP32	2500	Industrial grade -40℃~105℃
APM32F051K8T7-R	64	8	LQFP32	2000	Industrial grade -40℃~105℃
APM32F051K8T7	64	8	LQFP32	2500	Industrial grade -40℃~105℃
APM32F051C6T7-R	32	8	LQFP48	2000	Industrial grade -40℃~105℃
APM32F051C6T7	32	8	LQFP48	2500	Industrial grade -40℃~105℃
APM32F051C8T7-R	64	8	LQFP48	2000	Industrial grade -40℃~105℃
APM32F051C8T7	64	8	LQFP48	2500	Industrial grade -40℃~105℃
APM32F051R6T7-R	32	8	LQFP64	1000	Industrial grade -40℃~105℃
APM32F051R6T7	32	8	LQFP64	1600	Industrial grade -40℃~105℃
APM32F051R8T7-R	64	8	LQFP64	1000	Industrial grade -40℃~105℃
APM32F051R8T7	64	8	LQFP64	1600	Industrial grade -40℃~105℃

Note :SPQ= Smallest Packaging Quantity

8 Packaging Information

8.1 Reel Packaging

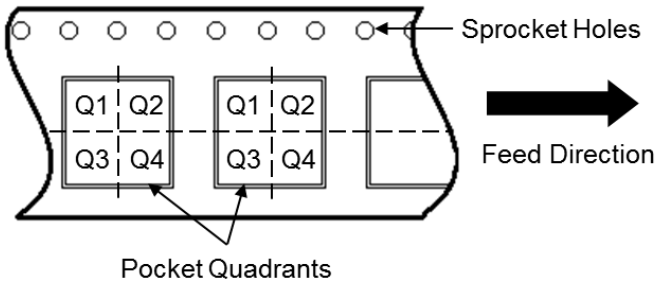
Figure 32 Specification Drawing of Reel Packaging



A0	Dimension designed to accommodate the component width

B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions

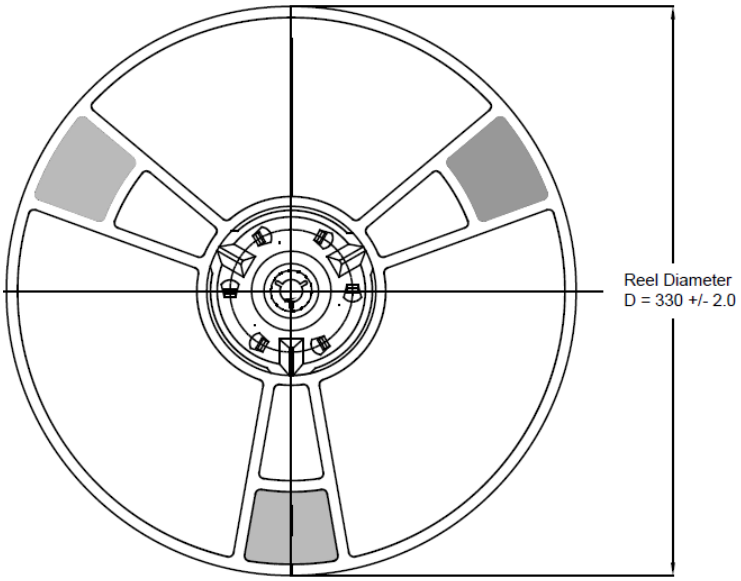
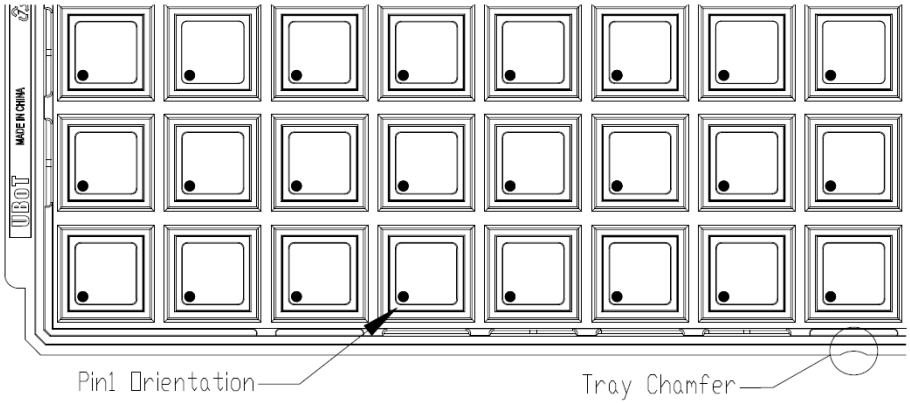


Table 58 Reel Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
APM32F051R6T6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F051R8T6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F051C6T6	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
APM32F051C8T6	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
APM32F051K6T6	LQFP	32	2000	330	9.3	9.3	2.2	16	Q1
APM32F051K8T6	LQFP	32	2000	330	9.3	9.3	2.2	16	Q1
APM32F051C6U6	QFN	48	2500	330	7.4	7.4	1.4	16	Q1
APM32F051C8U6	QFN	48	2500	330	7.4	7.4	1.4	16	Q1
APM32F051K6U6	QFN	32	5000	330	5.3	5.3	0.8	12	Q1
APM32F051K8U6	QFN	32	5000	330	5.3	5.3	0.8	12	Q1
APM32F051R6T7	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F051R8T7	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F051C6T7	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
APM32F051C8T7	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
APM32F051K6T7	LQFP	32	2000	330	9.3	9.3	2.2	16	Q1
APM32F051K8T7	LQFP	32	2000	330	9.3	9.3	2.2	16	Q1
APM32F051C6U7	QFN	48	2500	330	7.4	7.4	1.4	16	Q1
APM32F051C8U7	QFN	48	2500	330	7.4	7.4	1.4	16	Q1
APM32F051K6U7	QFN	32	5000	330	5.3	5.3	0.8	12	Q1
APM32F051K8U7	QFN	32	5000	330	5.3	5.3	0.8	12	Q1

8.2 Tray packaging

Figure 33 Tray Packaging Diagram



Tray Dimensions

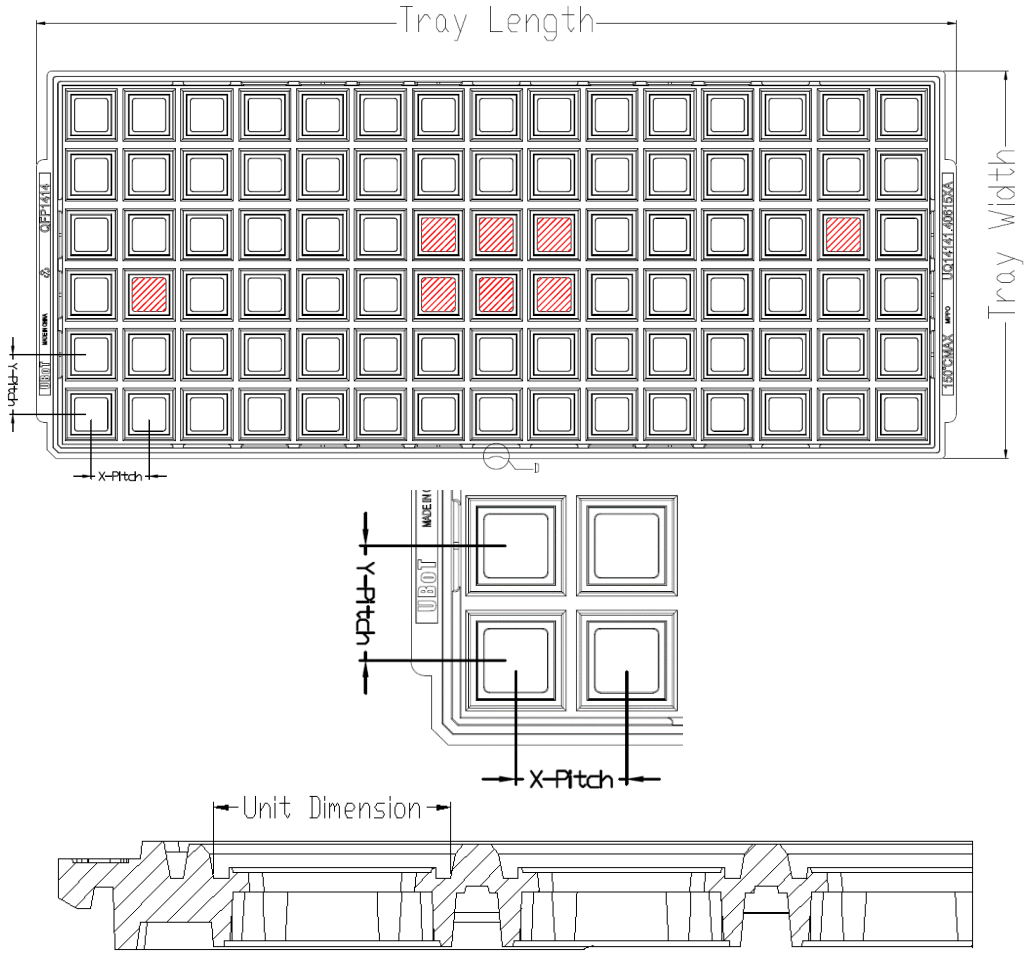


Table 59 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
APM32F051R6T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F051R8T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F051C6T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F051C8T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F051K6T6	LQFP	32	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F051K8T6	LQFP	32	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F051C6U6	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9
APM32F051C8U6	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9
APM32F051K6U6	QFN	32	4900	5.2	5.2	8.7	9.0	322.6	135.9
APM32F051K8U6	QFN	32	4900	5.2	5.2	8.7	9.0	322.6	135.9
APM32F051R6T7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F051R8T7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F051C6T7	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
APM32F051C8T7	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F051K6T7	LQFP	32	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F051K8T7	LQFP	32	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F051C6U7	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9
APM32F051C8U7	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9
APM32F051K6U7	QFN	32	4900	5.2	5.2	8.7	9.0	322.6	135.9
APM32F051K8U7	QFN	32	4900	5.2	5.2	8.7	9.0	322.6	135.9

9 Commonly Used Function Module Denomination

Table 60 Commonly Used Function Module Denomination

Full name	Short name
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External interrupt	EINT
Genera-purpose IO	GPIO
Alternate function IO	AFIO
Wake up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
External memory controller	EMMC
Controller local area network	CAN
I2C interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC

10 Version History

Table 61 Document Revision History

Date	Version	Change History
October 22, 2020	V1.0.	New
February 20, 2021	V1.1	(1) Modify HXT-HSECLK LXT-LSECLK HIRC-HSICLK LIRC-LSICLK (2) Delete 051 small-capacity content
March 29, 2021	V1.2	Modify th ($_{SDA}$) data in "Table 45 I2C Interface Characteristics"
June 4,2021	V1.3	(1) Modify low speed external clocks to LSECLK (2) Delete the temperature sensor module (3) Modify the header cover, and Package logo
June 30,2021	V1.4	Increase the maximum rated current characteristic
April 8, 2022	V1.5	Modify the unit of Peripheral power consumption
June 22,2022	V1.6	(1) Modify Arm trademark (2) Add the statement (3) Modify product naming rules figure
October, 2024	V1.7	(1) Modify the content of the touch sensing controller (2) Add flash storage time and erase cycle
June, 2025	V1.8	Add power-on/power-off characteristics

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